CML Microcircuits
COMMUNICATION SEMICONDUCTORS

CMX869A
Low Power V.32 bis Modem with Auto / Manual Connect

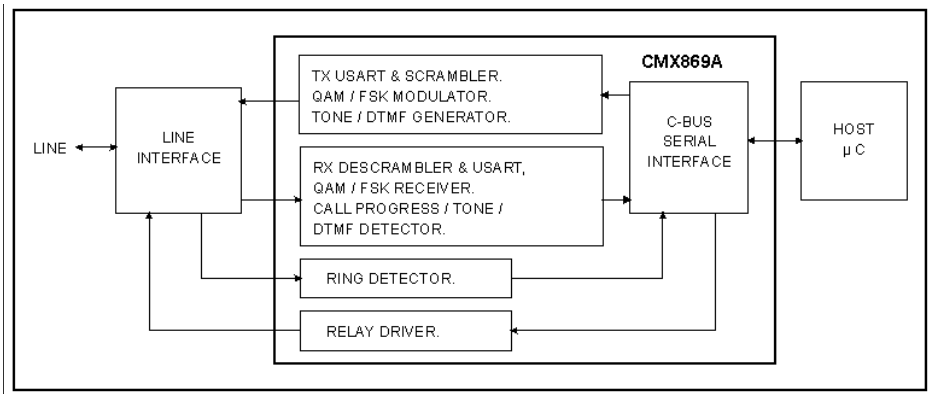
D/869A/2 August 2005 Provisional Issue

Features

- **V.32 bis/V.32/V.22 bis/V.22 Automodem (14400, 12000, 9600, 7200, 4800, 2400, 1200 bps Duplex)**
- **V.22 bis / V.22 Manual Modem (2400, 1200 bps)**
- **V.23 (1200/75, 1200/1200, 75, 1200 bps FSK)**
- **Bell 202 (1200/150, 1200/1200, 150, 1200 bps FSK)**
- **V.21 or Bell 103 (300/300 bps FSK)**
- **DTMF/Tones Transmit and Receive**
- **'Powersave' Standby Mode**
- **Asynchronous, Synchronous and HDLC Modes**

Applications

- **EPOS Terminals**
- **Telephone Telemetry Systems**
- **Remote Utility Meter Reading**
- **Security Systems**
- **Industrial Control Systems**
- **Electronic Cash Terminals**
- **Pay-Phones**
- **Cable TV Set-Top Boxes**



1. Brief Description

The CMX869A is a multi-standard modem for use in EPOS terminals, telephone based information and telemetry systems. It can transmit and detect standard DTMF and modem calling and answer signals or user-specific programmed single or dual tone signals. A general purpose Call Progress signal detector is also included. Flexible line driver and receive hybrid circuits are integrated on chip, requiring only passive external components to build a 2 or 4-wire line interface.

The device features a software controlled hook switch Relay Drive output and a Ring Detector circuit, which continue to function when the device is in Powersave mode. When a line voltage reversal or ringing signal is detected, the Ring Detector Circuit can provide an interrupt which can be used to wake up the host µController.

Control of the device is via a simple, high-speed serial bus that operates in normal and Powersave modes, which is compatible with most types of µC serial interface. The data transmitted and received by the modem is also transferred over the same serial bus. On-chip programmable Tx and Rx USARTs, compatible with V.14, are provided for use with asynchronous data and to allow unformatted synchronous data to be received or transmitted as 8-bit words or received as an HDLC packet.

The CMX869A operates from a single 3.3V supply over a temperature range of -40°C to +85°C and is available in 24-pin TSSOP (E2), SOIC (D2) and DIL (P4) packages.

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It is always recommended that you check for the latest product datasheet version from the Datasheets page of the CML website: [www.cmlmicro.com].

2. Block Diagram

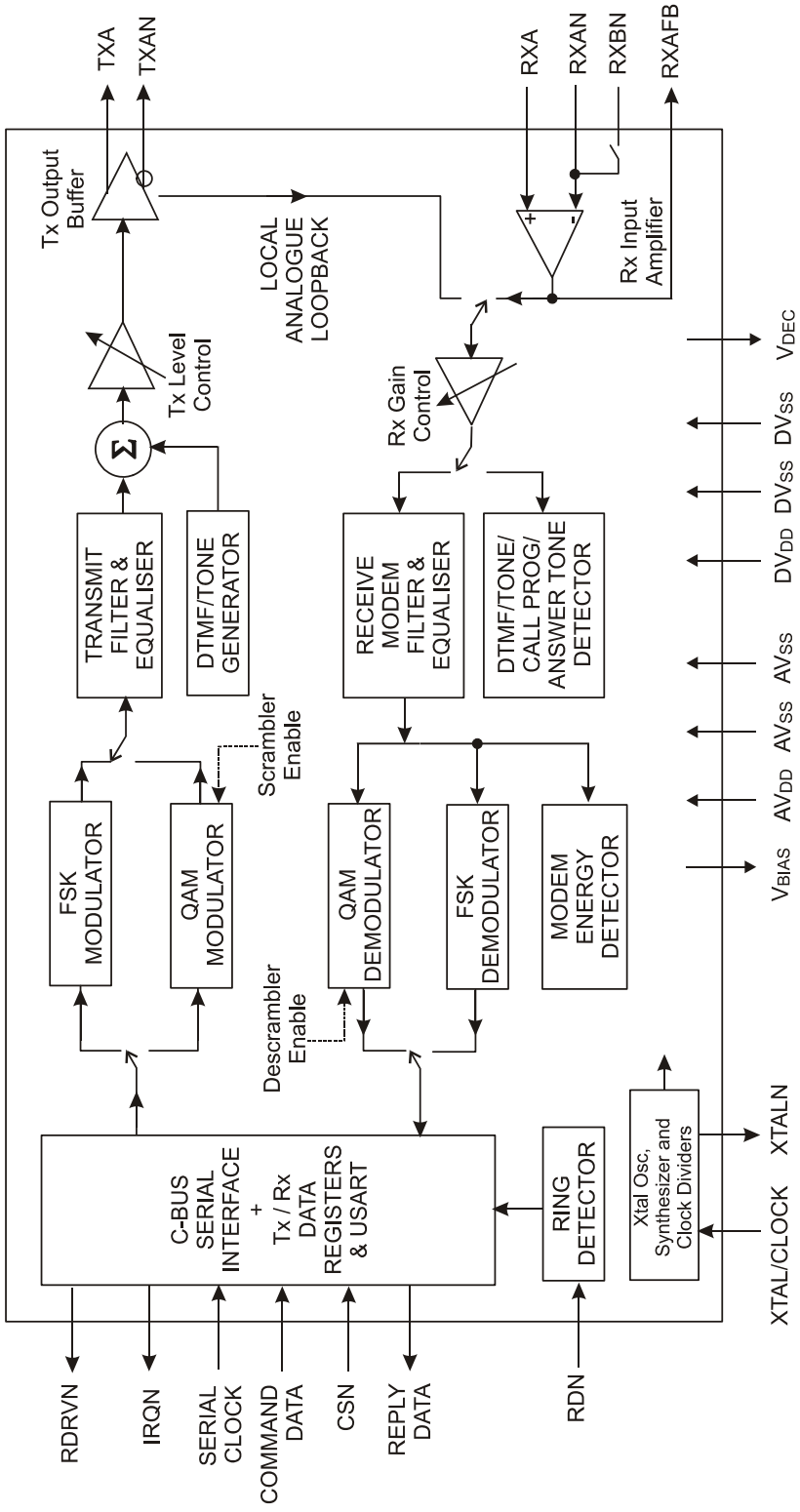


Figure 1 Block Diagram

3. Signal List

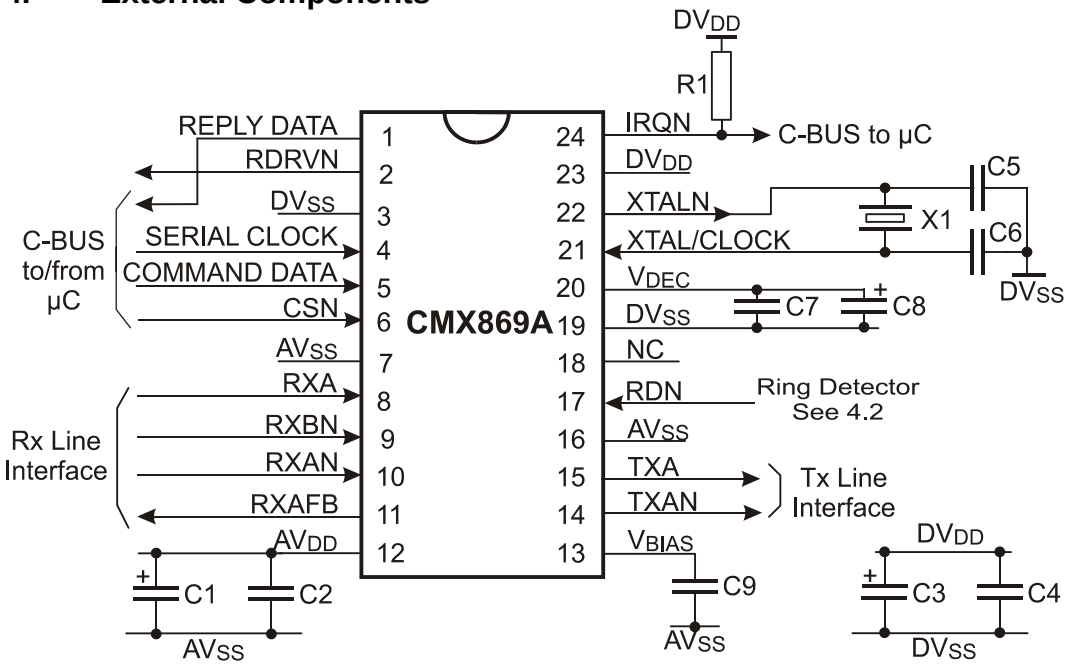
CMX869A D2/E2/P4	Signal		Description
Pin No.	**Name**	**Type**	
1	REPLY DATA	TS	A 3-state C-BUS serial data output to the μC. This output is high impedance when not sending data to the μC.
2	RDRVN	OP	Relay Drive output, low resistance pull down to V_{SS} when active and medium resistance pull up to V_{DD} when inactive.
4	SERIAL CLOCK	IP	The C-BUS serial clock input from the μC.
5	COMMAND DATA	IP	The C-BUS serial data input from the μC.
6	CSN	IP	The C-BUS chip select input from the μC.
8	RXA	IP	The non-inverting input to the Rx Input Amplifier
9	RXBN	IP	A second, switched inverting input to the Rx Input Amplifier. Used to increase the input stage gain. If not required, leave this pin unconnected.
10	RXAN	IP	The inverting input to the Rx Input Amplifier
11	RXAFB	OP	The output of the Rx Input Amplifier.
13	V_{BIAS}	OP	Internally generated bias voltage of approximately $AV_{DD}/2$, except when the device is in 'Powersave' mode when V_{BIAS} will discharge to AV_{SS}. Must be decoupled to AV_{SS} by a capacitor mounted close to the device pins.
14	TXAN	OP	The inverted output of the Tx Output Buffer.
15	TXA	OP	The non-inverted output of the Tx Output Buffer.
17	RDN	IP	Schmitt trigger input to the (inverting) Ring signal detector. Connect to DV_{DD} if Ring Detector is not used.
18	-	NC	Reserved for future use. Do not connect to this pin.
20	V_{DEC}	PWR/ OP	Internally generated 2.5V supply voltage. Must be decoupled to DV_{SS} by capacitors mounted close to the device pins. No other connections allowed.
21	XTAL/CLOCK	IP	The input to the oscillator inverter from the Xtal circuit or external clock source.
22	XTALN	OP	The output of the on-chip Xtal oscillator inverter.
24	IRQN	OP	A 'wire-ORable' output for connection to a μC Interrupt Request input. This output is pulled down to DV_{SS} when active and is high impedance when inactive. An external pullup resistor is required ie R1 of Figure 2

Signal list (cont.)

CMX869A D2/E2/P4	Signal		Description
Pin No.	**Name**	**Type**	
3, 19	DV_{SS}	PWR	The negative supply rail (ground) for the digital on-chip circuits.
7, 16	AV_{SS}	PWR	The negative supply rail (ground) for the analogue on-chip circuits.
12	AV_{DD}	PWR	The positive supply rail for the analogue on-chip circuits. Levels and thresholds within the device are proportional to this voltage.
23	DV_{DD}	PWR	The positive supply rail for the digital on-chip circuits.

Notes: IP = Input
OP = Output
TS = 3-state Output
PWR = Power
NC = No Connection

4. External Components



R1	100kΩ	C2, C4, C7, C9	100nF
X1	6.144MHz	C5, C6	47pF (see text)
C1, C3, C8	10uF		

Resistors ±5%, capacitors ±20% unless otherwise stated.

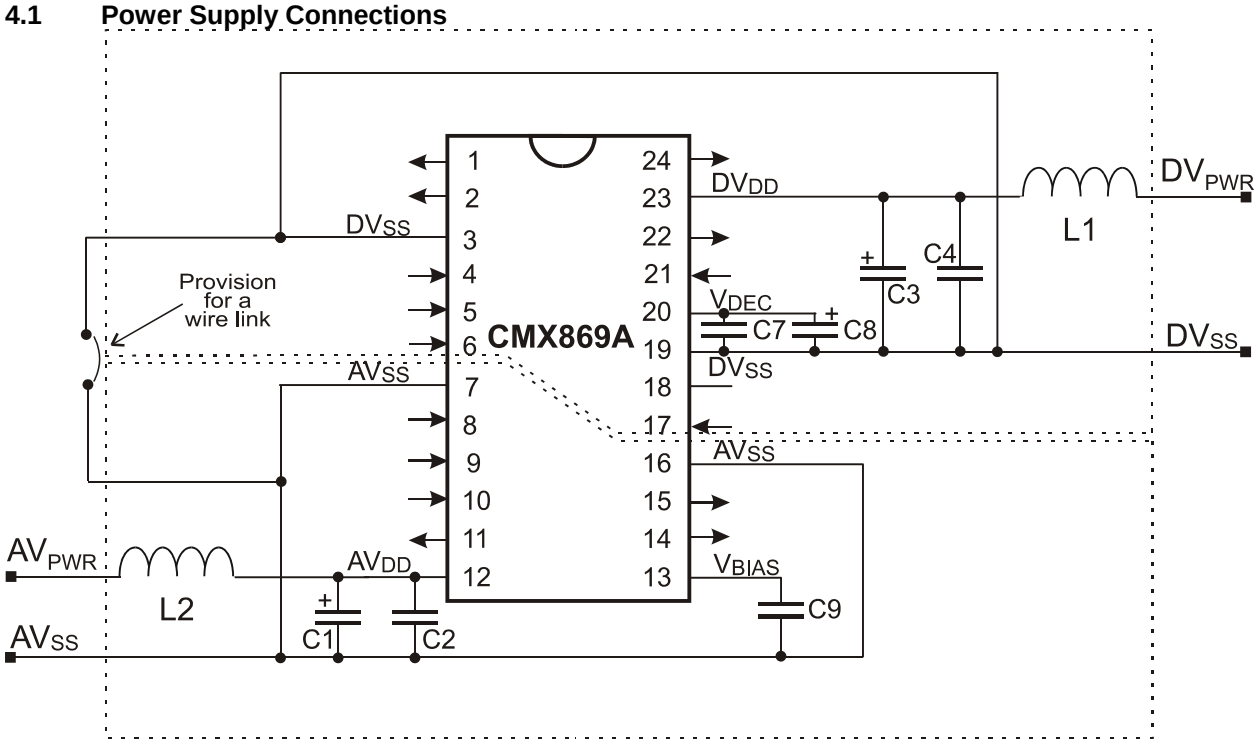
Figure 2a Recommended External Components for a Typical Application

This device is capable of detecting and decoding small amplitude signals. To achieve this DV_{DD}, AV_{DD} and V_{BIAS} should be decoupled and the receive path protected from extraneous in-band signals. It is recommended that the printed circuit board is laid out with both AV_{SS} and DV_{SS} ground planes in the CMX869A area, as shown in Figure 2b, with provision to make a link between them close to the CMX869A. To provide a low impedance connection to ground, the decoupling capacitors (C1 – C4, C7, C8) must be mounted as close to the CMX869A as possible and connected directly to their respective ground plane. This will be achieved more easily by using surface mounted capacitors.

V_{BIAS} is used as an internal reference for detecting and generating the various analogue signals. It must be carefully decoupled, to ensure its integrity. If V_{BIAS} needs to be used (other than as shown in figures 4a or 4b) to set external analogue levels, it must be buffered with a high input impedance buffer.

The values for capacitors C5 and C6 are suggestions for use with many typical crystals. However, the values of these capacitors must be chosen to comply with the crystal manufacturer's specification to ensure that the clock accuracy is within 50ppm. The DV_{SS} connections to the Xtal oscillator capacitors C5 and C6 should also be of low impedance and preferably be part of the DV_{SS} ground plane to ensure reliable start up of the oscillator.

4.1 Power Supply Connections



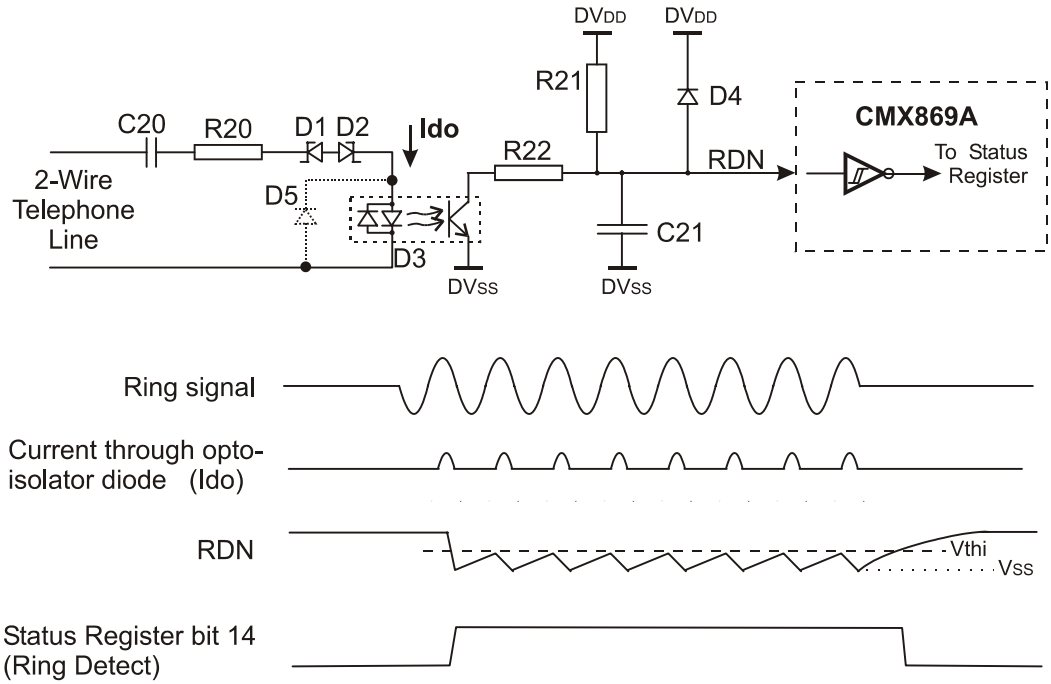
	ANALOGUE		DIGITAL
C2, C9	100nF	C4, C7	100nF
C1	10uF	C3, C8	10uF
L2	100nH (optional)	L1	100nH (optional)

Figure 2b Recommended Power Supply Connections and De-coupling

The inductors L1 and L2 can be omitted but this may degrade system performance.

Ensure that the length of the tracks between capacitors C2, C4, C7 and C9 and their corresponding CMX869A device pins (pins 12, 23, 20 and 13) are kept as short as possible.

4.2 Ring Detector Interface



R20	10kΩ, 0.5W	C21	0.33μF
R21	470kΩ	D1, D2	18V zener
R22	100Ω	D3	Opto isolator (NEC PS2701-1)
C20	0.33μF, 250V	D4	1N4004

Resistors ±5%, capacitors ±20%. Typical circuit, component types and values.

Figure 3 Ring Signal Detector Interface Circuit

Figure 3 shows how the CMX869A may be used to detect the large amplitude Ringing signal voltage present on the 2-wire line at the start of an incoming telephone call. The ring signal is usually applied at the subscriber's exchange as an ac voltage inserted in series with one of the telephone wires and will pass through C20, R20, D1 and D2, and appear at the terminals of D3. When the signal reaches the zeners' (D1, D2) turn-on voltage, current will flow into the opto-isolator diode, turning on its output transistor and discharging capacitor C21. Resistor R22 limits the current drawn by the opto-isolator output to ~30mA peak. Whilst the ring tone is active and exceeds the zener voltage, the RDN node will be taken low and the output of the Schmitt trigger will go high. The state of bit 14 (Ring Detect) of the Status Register directly corresponds to the state of the Ring Detect Schmitt trigger output. If the corresponding interrupt mask bit is set to 1, a C-BUS interrupt will be initiated (see the Status Register description in section 6.8). Note that the opto-coupler diode (D3) must be protected by a reverse voltage diode. If this is not available in the package, then an external 1N4148 (D5) may be fitted (as shown).

The minimum amplitude ringing signal that is certain to be detected is: $V_{zener} + V_{diode} + V_{opto} + 2V$.

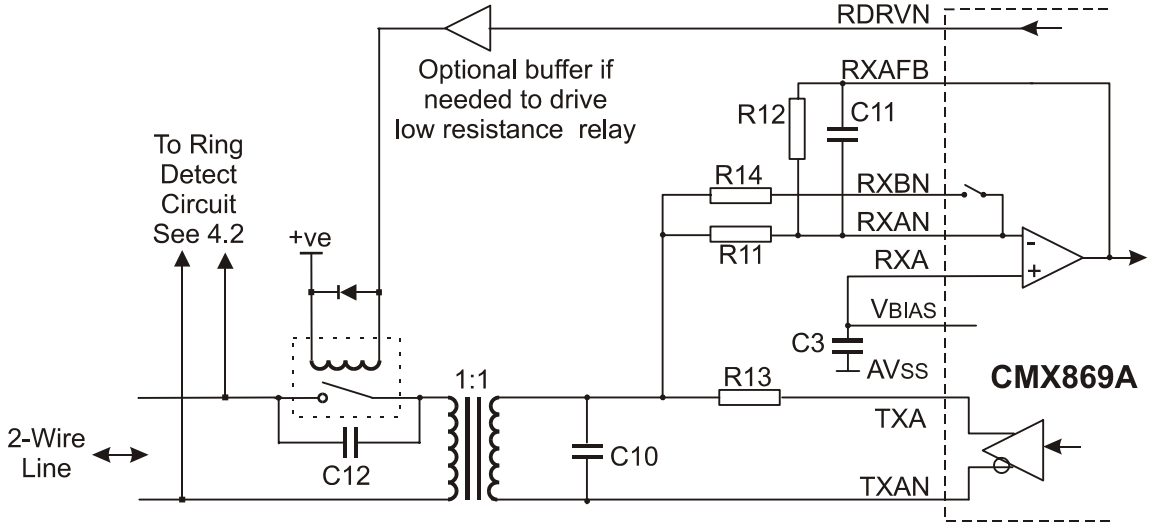
This requirement is met (with margin) by ringing signals of 40Vrms or above, for DVdd over the range 3.0 to 3.6V.

4.3 Line Interface

A line interface circuit is needed to provide dc isolation and to terminate the line. The CMX869A is connected to the line when the line relay is closed. The relay may be driven from the RDRVN output, as shown in figure 4a. Control of the output level of the RDRVN pin is described in section 6.2. The diagrams of Figure 4a and Figure 4b are functional representations only and should not be used in product designs. A reference design will be available separately.

2-Wire Line Interface

Figure 4a shows a simplified interface for use with a 600Ω 2-wire line. The line termination impedance is provided by the transformer, R13 and C10, high frequency noise is attenuated by C10 and C11, while R11 and R12 set the receive signal level into the modem. For clarity the 2-wire line protection circuits have not been shown.



R11	130kΩ (see text)	C3	See Figure 2
R12	100kΩ	C10	33nF
R13	600Ω	C11	100pF
R14	15kΩ (see text)	C12	100nF, 250V (see text)

Resistors ±5%, capacitors ±20%

Figure 4a 2-Wire Line Interface Circuit

The transmit line signal level is determined by the voltage swing between the TXA and TXAN pins, less 6dB due to the line termination resistor R13, and less the loss in the line coupling transformer. Allowing for 1dB loss in the transformer, with the Tx Mode Register set for a Tx Level Control gain of 0dB the nominal transmit line levels will be:

	V_{DD} = 3.3V
QAM and FSK Tx modes (no guard tone)	-7.5 dBm
Single tone transmit mode	-7.5 dBm
DTMF transmit mode	-3.5 and -5.5 dBm

For a line impedance of 600Ω, 0dBm = 775mVrms. See also section 8.1.3

In the receive direction, the signal detection thresholds within the CMX869A are proportional to AV_{DD} and are affected by the Rx Gain Control gain setting in the Rx Mode Register. The signal level into the CMX869A is affected by the line coupling transformer loss and the values of R11 and R12 of Figure 4a.

The value of R11 should be chosen so that the received signal level at the RXAFB pin is 3.6dB lower than that on the 2-wire line. For example if the transformer loss is 1dB then R11 should be 130kΩ. The value of

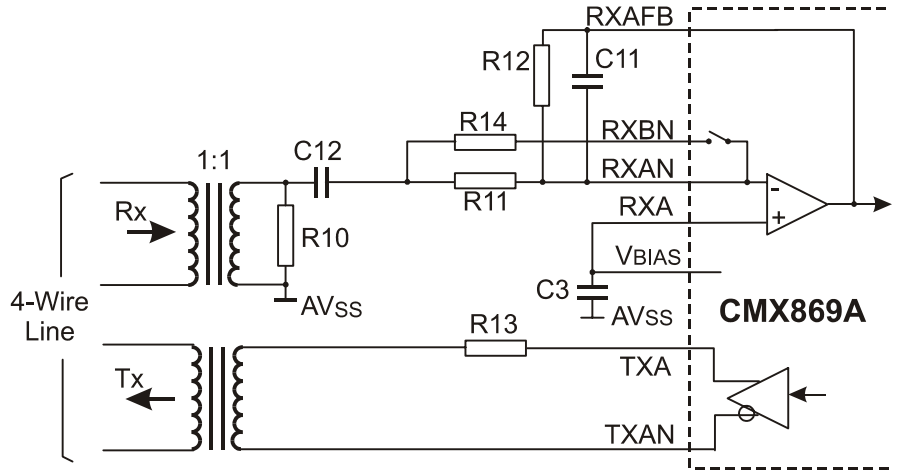
R14 (15kΩ) is chosen to apply approximately 20dB of extra gain, when required by Type 1 Caller Line Identification.

For best Rx performance, it is recommended that the transformer coupling arrangement should provide at least 7dB trans-hybrid loss.

The RXBN input can be selected by setting bit 14 of the General Control Register to 1, which internally connects RXBN to RXAN. With the components shown in Figures 4a and 4b, this will add approximately 20dB to the Rx gain, by connecting R14 in parallel with R11. This facilitates detection of certain signals whilst on-hook, such as may be required for Type 1 Caller Line Identification reception. For the 2-wire line interface shown in Figure 4a, capacitor C12 is required to provide an AC path through to the device when the relay is open. If this facility is not required, R14 and C12 can be omitted.

4-Wire Line Interface

Figure 4b shows a simplified interface for use with a 600Ω 4-wire line. The line terminations are provided by R10 and R13, high frequency noise is attenuated by C11 while R11 and R12 set the receive signal level into the modem. Transmit and receive line level settings and the values of R11 and R14 are as for the 2-wire circuit.



R10, 13	600Ω	C3	See Figure 2
R11	130kΩ (see text)	C11	100pF
R12	100kΩ	C12	33nF
R14	15kΩ (see text)		

Resistors ±5%, capacitors ±20%

Figure 4b 4-Wire Line Interface Circuit

5. General Description

The CMX869A can operate as a full duplex QAM (Quadrature Amplitude Modulation) or DPSK (Differential Phase Shift Keying) Automodem, using the following modulation schemes:

- V.32bis
- V.32
- V.22bis
- V.22

with data rates of 14400, 12000, 9600, 7200, 4800, 2400 or 1200bps.

Note: reference to QAM elsewhere in the datasheet implies QAM or DPSK, according to selected operating mode.

It can also be set to operate under host control of the connection sequence in the following low speed modem modes:

- V.22bis
- V.22
- V.21 or Bell 103. 300/300bps duplex FSK (Frequency Shift Keying).
- V.23 modem. 1200 or 75 bps FSK.
- Bell 202 modem. 1200 or 150 bps FSK.

The transmit circuits can also be set to any one of the following:

- DTMF transmit.
- Single tone transmit (from a range of modem calling, answer and other tone frequencies)
- User programmed tone or tone pair transmit (programmable frequencies and levels)
- Disabled.

The receive circuits can also be set to:

- DTMF detect.
- 2100Hz and 2225Hz answer tone detect.
- Call progress signal detect.
- User programmed tone or tone pair detect.
- Disabled.

The Ring Detect, Tone Decoder and FSK modem circuits can be configured to facilitate Type 1 (On-Hook) Caller Identification. This facility is the subject of separate application notes.

When not in use, the CMX869A may be set into a Powersave mode, which disables all circuitry except for the on-chip regulator, the C-BUS interface and the Ring Detector.

5.1 Tx USART

A flexible Tx USART is provided for all modem modes, designed to meet the requirements of V.14. It can be programmed to transmit continuous patterns, Start-Stop characters or Synchronous unformatted data.

The data to be transmitted is written by the µC into the C-BUS Tx Data Register ($E3). The Tx and Rx Data Register can be set to operate in 8 or 16-bit mode by setting the General Control Register b10 appropriately at power-on.

Synchronous mode
If Synchronous Data mode has been selected the 8 data bits of each octet in the Tx Data Buffer are transmitted serially, the lsb being sent first. The last transmitted byte will be re-transmitted if there is no new data in the Transmit Data Register

Stop-Start (Asynchronous) mode
In Start-Stop mode an asynchronous character is transmitted for each octet in the Tx Data Register. Each character consists of a single Start bit followed by 5, 6, 7 or 8 data bits from the Tx Data Buffer - lsb first - followed by an optional Parity bit then - normally - one or two Stop bits. The Start, Parity and Stop bits are generated by the USART as determined by the Tx Mode Register settings and are not taken from the Tx Data Register. A continuous Stop signal (1) will be transmitted if there is no new data in the Transmit Data Register.

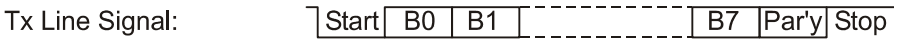


Figure 5a Tx USART Output: Start-Stop mode, 8 Data Bits + Parity

16 bit (2-Character mode)
In 16-bit (2 character) mode data written to the Tx Data Register at C-BUS address $E3 will be treated as two octets, b15-8 which will be transmitted first and b7-0 which will be transmitted second. If there is a need to transmit a single octet when the Tx Data Register has been set to 16-bit mode this can be achieved by writing the 8-bit data to C-BUS address $E4 instead of $E3.

If the Tx Data Register has been set to operate in 8-bit (1 character) mode, data should be written to C-BUS address $E3, address $E4 being used to provide for Start-Stop transmit data overspeed as described later.

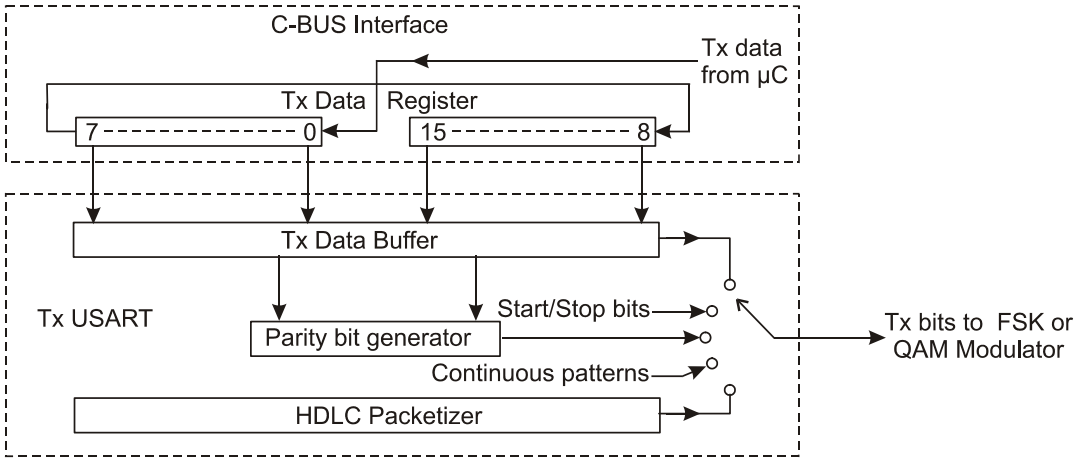


Figure 5c Tx USART (in 16 Bit Mode)

Status Register, Tx Data Ready and Tx Data Underflow bits
Every time the contents of the C-BUS Tx Data Register have been transferred to the Tx Data Buffer the Tx Data Ready flag bit of the Status Register is set to 1 to indicate that new data should be loaded into the C-BUS Tx Data Register. This flag bit will be cleared to 0 when a new value is loaded into the Tx Data Register.

If a new value is not loaded into the Tx Data Register in time for the next Tx Data Register to Tx Data Buffer transfer then the Status Register Tx Data Underflow bit will be set to 1

V.14 and Overspeed operation

In all modes the transmitted bit and baud rates are the nominal rates for the selected modem type, with an accuracy determined by the XTAL frequency accuracy, however V.14 requires that Start-Stop characters can be transmitted at up to 1% overspeed (basic signalling rate range) or 2.3% overspeed (extended signalling rate range) by deleting a Stop bit from no more than one out of every 8 (basic range) or 4 (extended range) consecutive transmitted characters.

To accommodate this V.14 requirement the CMX869A allows the controlling µC to reduce the number of transmitted Stop bits by one for selected characters in QAM Start-Stop modes. To do this, the device must be set to operate in 1 character mode for the entire transmission by clearing General Control Register b10 to 0 (note: the bit is only actioned following a reset or power-on). Characters written to thc C-BUS Tx Data Register at address $E3 will then be transmitted with the programmed number of Stop bits, but a character written to $E4 will be transmitted with one less Stop bit than the number programmed in the Tx Mode Register.

In FSK Start-Stop modes, if the device is set for 1 character mode (General Control Register b10 = 0) data written to $E4 will be transmitted with a 12.5% reduction in the length of the Stop bit at the end of that character. In all 8 bit Synchronous Data modes data, written to $E4 will be treated as though it had been written to $E3. The behaviour is not defined for 16 bit data mode.

The underspeed transmission requirement of V.14 is automatically met by the CMX869A, as in Start-Stop mode it will insert extra Stop bit(s) if it has to wait for new data to be loaded into the C-BUS Tx Data Register.

Data Scramblers

The QAM (V.32bis/V.32/V.22bis/V.22) modulators include compatible data scrambler functions that are automatically enabled as required in AutoModem modes or may be manually controlled in V.22 bis and V.22 manual operation from the Tx and Rx mode registers.

5.2 FSK and QAM Modulators

Serial data from the USART is fed to the FSK modulator if V.21, V.23, Bell 103 or Bell 202 mode has been selected, or to the QAM modulator for V.22bis, V.22, V.32bis and V.32 modes.

The FSK modulator generates one of two frequencies according to the transmit mode and the value of current transmit data bit.

In V.22bis and V.22 modes, QAM modulation is applied to a carrier of 1200Hz (Low Band, Calling modem) or 2400Hz (High Band, Answering modem).

In V.32bis and V.32 modes, QAM modulation is applied to a carrier of 1800Hz, using Trellis encoding for most bit rates.

5.3 Tx Filter and Equaliser

The FSK or QAM/DPSK modulator output signal is fed through the Transmit Filter and Equaliser block which limits the out-of-band signal energy to acceptable limits. In 1200 and 2400 bps, DPSK and QAM manual modes this block includes a fixed compromise line equaliser which is automatically set for the particular modulation type and frequency band being employed. This fixed compromise line equaliser may be enabled or disabled by bit 15 of the General Control Register. The amount of Tx equalisation provided compensates for one quarter of the relative amplitude and delay distortion of ETS Test Line 1 over the frequency band used.
In Auto Modem modes, the appropriate equalisation for the particular operating mode is determined and selected automatically by the device.

5.4 DTMF/Tone Generator

In DTMF/Tones mode this block generates DTMF signals or single or dual frequency tones. In V.22 bis modem mode it is used to generate the optional 550Hz or 1800Hz guard tone.

5.5 Tx Level Control and Output Buffer

The outputs (if present) of the Transmit Filter and DTMF/Tone Generator are summed then passed through the programmable Tx Level Control (provides the ability to attenuate the transmitted signal by up to 10.5dB) and Tx Output Buffer to the pins TXA and TXAN. The Tx Output Buffer has symmetrical outputs to provide sufficient line voltage swing and to reduce harmonic distortion of the signal.

5.6 Rx Level Control

In normal (non loopback) mode, the output from the Rx Input Amplifier is fed to the Rx Gain Control block. This provides the ability to attenuate the received signal by up to 10.5dB, depending on the value programmed into the Receive Mode Register. The output from the Rx Gain Control block is routed either to the Modem functions or to the Tone Detectors.

5.7 Rx DTMF/Tones Detectors

In Rx Tones Detect mode the received signal, after passing through the Rx Gain Control block, is fed to the DTMF / Tones / Call Progress / Answer Tone Detector. The user may select any of four separate detectors:

The DTMF Detector detects standard DTMF signals and identifies the transmitted character in the Status Register. A valid DTMF signal will set bit 5 of the Status Register to 1 for as long as the signal is detected.

The Programmable Tone Pair Detector includes two separate tone detectors (see Figure 10). The first detector will set bit 6 of the Status Register for as long as a valid signal is detected, the second detector sets bit 7, and bit 10 of the Status Register will be set when both tones are detected.

The Call Progress Detector measures the amplitude of the signal at the output of a 275Hz - 665Hz bandpass filter and sets bit 10 of the Status Register to 1 when the signal level exceeds the measurement threshold. The response of the Call Progress filter, including the effect of external components of figures 4a and 4b, is shown in Figure 6.

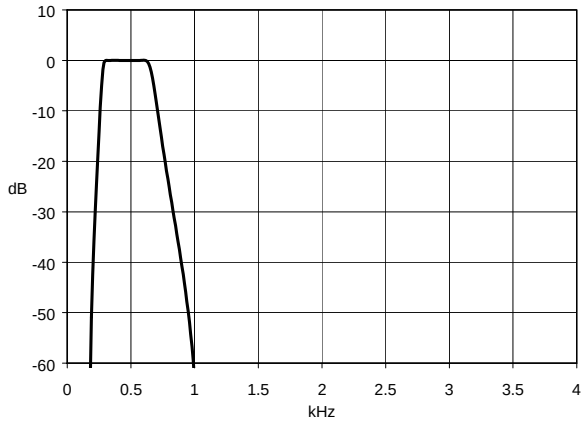


Figure 6 Response of Call Progress Filter

The Answer Tone Detector measures both amplitude and frequency of the received signal and sets bit 6 or bit 7 of the Status Register when a valid 2225Hz or 2100Hz signal is received.

5.8 Rx Modem Filtering and Demodulation

When the receive part of the CMX869A is operating as a modem, the received signal is fed through a bandpass filter to attenuate unwanted signals. The characteristics of the filter are determined by the chosen receive modem type and frequency band.

The output of the filter is fed to the appropriate FSK or QAM demodulator depending on the selected modem type:

In manual modem modes the signal level at the output of the Filter is also measured, compared to a threshold value, and the result controls bit 10 of the Status Register.

In QAM Auto Modem modes, a V.32 bis/V.32 echo canceller is included, which will work with a round trip delay of up to 1.25 seconds.

5.9 Rx Modem Pattern Detectors

In manual modem modes the received bit stream is monitored for continuous 1's, for continuous 0's, and for continuous alternating 1's and 0's. Bit 7, 8 or 9 of the Status Register will be set to 1 whenever 32 bits of the appropriate pattern has been received and will then remain at 1 for 12 bit times after the end of the detected pattern unless the receive operating mode is changed, in which case the pattern detectors are reset within 2 milliseconds.

In all modem modes a V.14 'Break' signal detector is implemented in Start-Stop mode by monitoring the received data and setting bit 8 of the Status Register when 2N + 4 consecutive 0's have been received, N being the total number of bits per character including the Start, Stop and any Parity bits.
The demodulated data is passed through a de-scrambler according to the requirements of the receiver operating mode. This function is enabled automatically, as required.

5.10 Rx USART

A flexible Rx USART is provided for all modem modes, meeting the requirements of V.14 for all modem speeds. Depending on the setting of the Rx Mode Register, it will treat the received data bit stream as Synchronous data, as Start-Stop characters or as HDLC Frames.

Synchronous mode

In Synchronous mode the received data bits are all fed into an internal Rx Data Buffer which is copied into the C-BUS Rx Data Register after every 8 or 16 bits, depending on the setting of the General Control Register '2 character mode' bit, b10.

Start-Stop (Asynchronous) mode

In Start-Stop mode the USART Control logic looks for the start of each character, then feeds only the required number of data bits (not parity) into an internal Rx Data Buffer. If the parity bit is used, both parity and the presence of a Stop bit are checked. Depending on the setting of b10 of the General Control Register, the data bits from 1 or 2 received characters are placed into the C-BUS Rx Data Register. If parity has been enabled the C-BUS Status Register 'Even Parity' bit(s) are set or cleared according to the received parity.

HDLC mode

In HDLC mode (algorithm based on BS 5397 Part 1 1985) the CMX869A recognises the start and end of an HDLC Frame by monitoring the received bit stream for the presence of the flag byte (01111110 binary). The received data and FCS octets within the Frame are then passed to the C-BUS Rx Data Register (one or two octets at a time depending on the setting of the '2-character' bit) after removal of any 'stuffed' 0's. A 16-bit Frame Check Sequence is calculated (as defined in RFC 1331) from the received data octets and compared to the received FCS at the end of the Frame, bit 4 of the Status Register being set to 1 if the two FCSs do not match. The 16 bit FCS data is output to the C-Bus Rx Data Register following the last data received.

16 bit (2-character mode)

If 2-character mode has been selected, received characters will normally be transferred to the C-BUS Rx Data Register two at a time and the Status Register b1 set to 1. However, the USART includes a time-out

function so that if a message contains an odd number of characters the final character will be transferred to the Rx Data Register and b1 of the Status Register will be cleared to '0'. This indicates that the next data to be read from the Rx Data Register holds the single last character in the least significant byte.

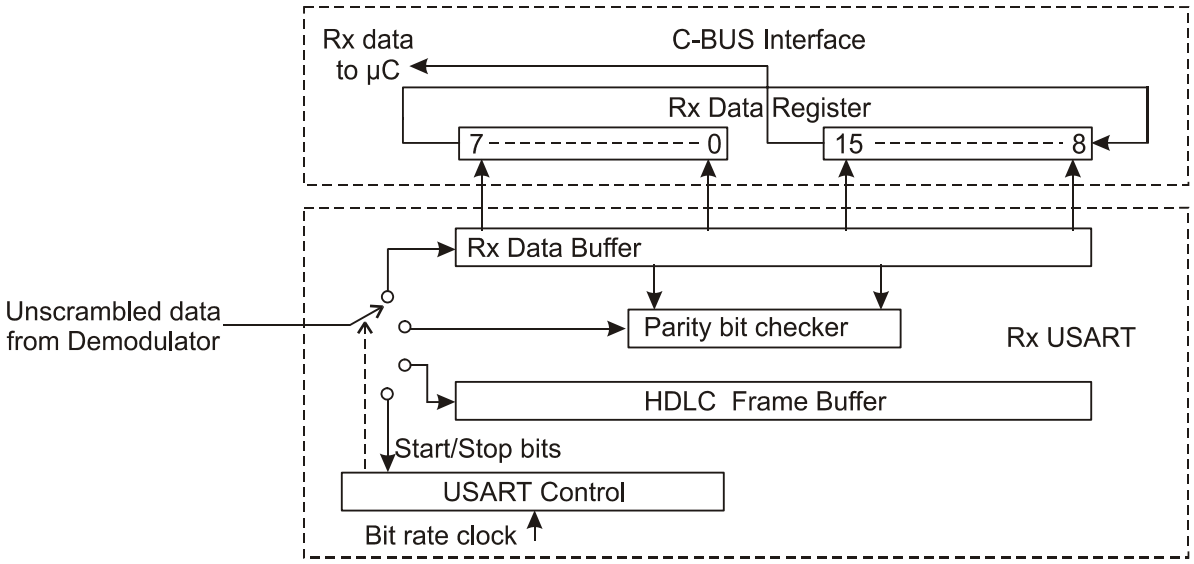


Figure 7 Rx USART (in 16 Bit Mode)

Status Register, Rx Data Ready and Rx Data Overflow bits
Whenever a new character or characters is copied into the C-BUS Rx Data Register, the Rx Data Ready flag bit b6 of the Status Register is set to '1' to prompt the µC to read the new data.

If the µC has not read the previous data from the Rx Data Register by the time that the CMX869A places fresh data into it, the Rx Data Overflow flag bit, b5 of the Status Register, will be set to 1.

The Rx Data Ready flag and Rx Data Overflow bits are cleared to 0 when the Rx Data Register is read by the µC.

V.14 operation and Overspeed (in Asynchronous mode)
If the Stop bit is missing at the end of a character (a '0' received instead of a '1') the received character will still be placed into the C-BUS Rx Data Register, but unless allowed by the V.14 overspeed option (see below), the Status Register Rx Framing Error bit (b4) will be set to '1' and the USART will re-synchronise onto the next '1' – '0' (Stop – Start) transition. [1]
The receive USART is able to cope with missing Stop bits; up to 1 missing Stop bit in every 8 consecutive received characters being allowed for the +1% overspeed (basic signalling rate) V.14 mode and 1 in 4 for the +2.3% overspeed (extended signalling rate) mode.

The CMX869A Rx Mode Register can be set for 0, +1% or +2.3% overspeed operation. Missing Stop bits beyond those allowed by the selected overspeed option will set the Rx Framing Error flag bit of the Status Register.

[1] In overspeed mode, the parity detect function can report incorrect parity for the character following a missing stop bit.

6. C-BUS Interface and Software Description

This block provides for the transfer of data and control or status information between the CMX869A's internal registers and the µC over the C-BUS serial bus. Each transaction consists of a single Register Address byte sent from the µC which may be followed by one or more data bytes sent from the µC to be written into one of the CMX869A's Write Only Registers, or one or more bytes of data read out from one of the CMX869A's Read Only Registers, as illustrated in Figure 8.

Data sent from the µC on the Command Data line is clocked into the CMX869A on the rising edge of the Serial Clock input. Reply Data sent from the CMX869A to the µC is valid when the Serial Clock is high. The CSN line must be held low during a data transfer and kept high between transfers. The C-BUS interface is compatible with most common µC serial interfaces and may also be easily implemented with general purpose µC I/O pins controlled by a simple software routine. Figure 13 gives detailed C-BUS timing requirements.

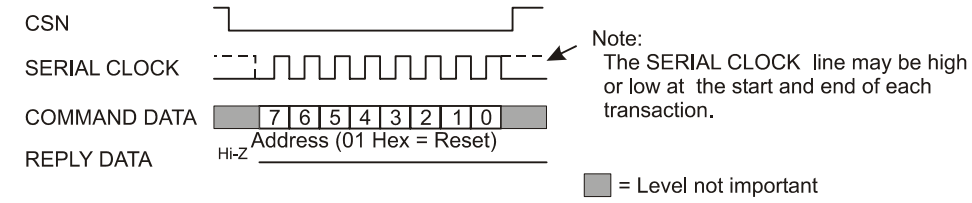
The following C-BUS addresses and registers are used by the CMX869A:

General Reset Command (address only, no data).	Address $01
General Control Register, 16-bit write only.	Address $E0
Transmit Mode Register, 16-bit write-only.	Address $E1
Receive Mode Register, 16-bit write-only.	Address $E2
Transmit Data Register, 8 or 16-bit write only.	Address $E3
Alternate Transmit Data Register, 8-bit write only.	Address $E4
Receive Data Register, 8 or 16-bit read-only.	Address $E5
Status Register, 16-bit read-only.	Address $E6
Programming Register, 16-bit write-only.	Address $E8
QAM Modem Command Register, 16-bit write-only.	Address $EA
QAM Modem Status Register, 16-bit read-only.	Address $EB

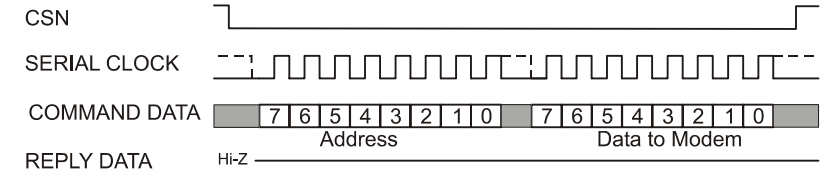
Note: The C-BUS addresses $E7, $E9, $EC, $ED, $EE and $EF are allocated for production testing and should not be accessed in normal operation.

Interrupt Operation
The CMX869A will issue an interrupt, by taking the IRQN line low, when the IRQ bit 15 of the Status Register and the IRQ Enable bit 6 in the General Control Register are both set = 1. The IRQ bit operation is described in section 6.8.

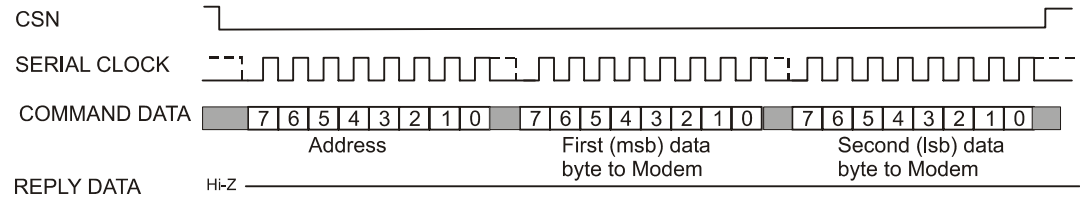
a) Single byte from µC (General Reset command)



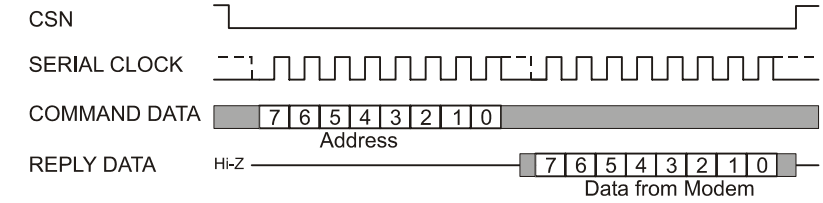
b) One Address and one Data byte from µC to Modem



c) One Address and 2 Data bytes from µC to Modem



d) One Address byte from µC and one Reply byte from Modem



e) One Address byte from µC and 2 Reply bytes from Modem

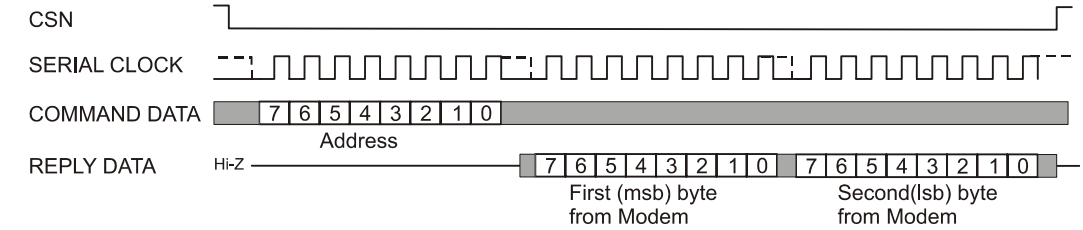


Figure 8 C-BUS Transactions

6.1 General Reset Command

General Reset Command (no data) C-BUS address $01

This command resets the device, clears all bits of the General Control, Transmit Mode and Receive Mode Registers as well as bits 15 and 13-0 of the Status Register and places the device into Powersave mode.

Whenever power is applied to the CMX869A, a built in power-on-reset circuit ensures that the device powers up into the same state as follows a General Reset command. Nevertheless, it is recommended that a General Reset command be sent to the device on power-up, after which the General Control Register should be set as required.

6.2 General Control Register

General Control Register: 16-bit write-only. C-BUS address $E0

This register controls general features of the CMX869A, such as the Powersave and Loopback modes, the IRQ mask bits and the Relay Drive output.

All bits of this register are cleared to 0 by a General Reset command. Note that the 2-character (2C) mode flag is **only** read following a reset or power-on.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Equ	Hi Gain	0	0	LB	2C	Rly drv	Pwr	Rst	Irqn en	IRQ Mask Bits					

General Control Register b15: Tx and Rx Fixed Compromise Equalisers
This bit allows the Tx and Rx fixed compromise equalisers in the modem transmit and receive filter blocks to be disabled in FSK/DPSK/QAM manual modem modes.

b15 = 1	Disable equalisers
b15 = 0	Enable equalisers (1200 or 2400bps modem modes)

General Control Register b14: Select high input gain
This bit selects the RXBN input pin and is used to increase the input stage gain.

b14 = 1	RXBN internally connected to RXAN
b14 = 0	RXBN open circuit

General Control Register b13,12: Reserved, set to 00

General Control Register b11: Analogue Loopback test mode
This bit controls the analogue loopback test mode. In loopback test mode both Transmit and Receive Mode Registers should be set to the same modem type, band and bit rate. The line interface relay must be open, as the test transmission that is fed back into the Rx path will appear at the Tx pins. Analogue loopback is not available in QAM Auto modem modes.

b11 = 1	Local analogue loopback mode enabled
b11 = 0	No loopback (normal modem operation)

General Control Register b10: Modem 2-Character mode
Selects whether the Tx Data and Rx Data Registers operate in 1 or 2 character mode.

b10 = 1	2 character mode
b10 = 0	1 character mode

The character mode is only updated on exit from a General Control initated reset, so General Control Register b7 (Power-up) must be set (written = 1) then cleared (written = 0), in conjunction with setting the desired character mode. Note that V.14 overspeed operation is NOT available in 2 character mode.

General Control Register b9: Relay Drive
This bit directly controls the RDRVN output pin.

b9 = 1	RDRVN output pin pulled to V_{SS}
b9 = 0	RDRVN output pin pulled to V_{DD}

General Control Register b8: Power-up
This bit controls the internal power supply to most of the internal circuits, including the Xtal oscillator, internal clock synthesizer and V_{BIAS} supply. Note that the General Reset command clears this bit, putting the device into Powersave mode.

b8 = 1	Device powered up normally
b8 = 0	Powersave mode (all circuits disabled, except the on-chip regulator, Ring Detect, RDRVN and C-BUS interface)

When power is first applied to the device, the following power-up procedure should be followed to ensure correct operation.

i. (Power is applied to the device)
ii. Issue a General Reset command.
iii. Write to the General Control Register (address $E0 setting both the Power-up bit (b8) and the reset bit (b7) to 1 – leave in this state for a minimum of about 20ms – this is required to ensure that the crystal oscillator, on-chip regulator and the V_{BIAS} supply are all operating prior to running any transmit or receive functions
iv. The device is now ready to be programmed as and when required. Examples:
- A General Reset command could be issued to clear all the registers and therefore powersave the device.
- The Reset bit in the General Control Register could be set to 0 as part of a routine to program all the relevant registers for setting up a particular operating mode.

When the device is switched from Powersave mode to normal operation by setting the Power-up bit to 1, the Reset bit should also be set to 1 and should be held at 1 for about 20ms while the on-chip regulator, crystal oscillator, clock synthesizer and V_{BIAS} stabilise before starting to use the transmitter or receiver.

General Control Register b7: Reset
Setting this bit to 1 resets the CMX869A's internal circuitry, clearing all bits of the Transmit Mode, Receive Mode, QAM Modem Control and Programming Registers and b13-0 of the Status Register.

b7 = 1	Internal circuitry in a reset condition.
b7 = 0	Normal operation

General Control Register b6: IRQNEN (IRQN O/P Enable)
Setting this bit to 1 enables the IRQN output pin.

b6 = 1	IRQN pin driven low (to V_{SS}) if the IRQ bit of the Status Register = 1
b6 = 0	IRQN pin disabled (high impedance)

General Control Register b5-0: IRQ Mask bits
These bits affect the operation of the IRQ bit of the Status Register as described in section 6.8

6.3 Transmit Mode Register

Transmit Mode Register: 16-bit write-only. C-BUS address $E1

This register controls the CMX869A transmit signal type and level. All bits of this register are cleared to 0 by a General Reset command or when b7 (Reset) of the General Control Register is 1.

Bit:

15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Tx mode = modem				Tx level			Guard tone		Scrambler		Start-stop / synch data		# data bits / synch data source		
Tx mode = DTMF/Tones				Tx level			0	DTMF twist			DTMF or Tone select				
Tx mode = Disabled				Set to 0000 0000 0000											

Tx Mode Register b15-12: Tx mode

These 4 bits select the transmit operating mode.

b15	b14	b13	b12		
1	1	1	1	V.22, V.22 bis, V.32, V.32 bis	QAM AUTO modem
1	1	1	0	Reserved, do not use	
1	1	0	1	V.22 bis 2400	High band (Answering modem)
1	1	0	0	V.22bis 2400	Low band (Calling modem)
1	0	1	1	V.22 1200	High band (Answering modem)
1	0	1	0	V.22 1200	Low band (Calling modem)
1	0	0	1	V.21 300 bps FSK	High band (Answering modem)
1	0	0	0	"	Low band (Calling modem)
0	1	1	1	Bell 103 300 bps FSK	High band (Answering modem)
0	1	1	0	"	Low band (Calling modem)
0	1	0	1	V.23 FSK	1200 bps
0	1	0	0	"	75 bps
0	0	1	1	Bell 202 FSK	1200 bps
0	0	1	0	"	150 bps
0	0	0	1	DTMF / Tones	
0	0	0	0	Transmitter disabled	

Tx Mode Register b11-9: Tx level

These 3 bits set the gain of the Tx Level Control block.

b11	b10	b9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Tx Mode Register b8-7: Tx Guard tone (V.22 bis mode)
These 2 bits select the guard tone to be transmitted together with the highband (answer) V.22 bis signal. Ignored in all other modes.

b8	b7	
1	1	Tx 550Hz guard tone
1	0	Tx 1800Hz guard tone
0	x	No Tx guard tone

Tx Mode Register b6-5: Tx Scrambler (QAM, DPSK manual modes)
These 2 bits control the operation of the Tx scrambler used in QAM and DPSK modes. Set both bits to 0 in FSK modes.

b6	b5	
1	1	Scrambler enabled, 64 ones detect circuit enabled (normal use)
1	0	Scrambler enabled, 64 ones detect circuit disabled
0	1	Reserved, do not use
0	0	Scrambler disabled

Tx Mode Register b4-3: Tx Modem Data format
These two bits select Special or Start-stop mode and the addition of a parity bit to transmitted characters in Start-stop mode.

b4	b3	
1	1	Special modes (see below)
1	0	Start-stop mode, no parity
0	1	Start-stop mode, even parity bit added to data bits
0	0	Start-stop mode, odd parity bit added to data bits

Tx Mode Register b2-0: Tx Modem Data and Stop bits (Start-Stop modes)
In Start-stop mode these three bits select the number of Tx data and stop bits.

b2	b1	b0	
1	1	1	8 data bits, 2 stop bits
1	1	0	8 data bits, 1 stop bit
1	0	1	7 data bits, 2 stop bits
1	0	0	7 data bits, 1 stop bit
0	1	1	6 data bits, 2 stop bits
0	1	0	6 data bits, 1 stop bit
0	0	1	5 data bits, 2 stop bits
0	0	0	5 data bits, 1 stop bit

Tx Mode Register b2-0: Tx Modem Data source (Special modes)
When b4-3 = 11 bits 2-0 select the source of the Transmitted data as below:

b2	b1	b0	
1	1	1	Synchronous , data bytes taken directly from the Tx Data Buffer
1	1	0	Reserved, do not use.
1	0	1	Reserved, do not use.
1	0	0	Reserved, do not use.
0	1	1	Continuous 1s
0	1	0	Continuous 0s
0	0	1	Continuous alternating 1s and 0s (or 11, 00 in V22 modes)
0	0	0	Reserved, do not use.

Tx Mode Register b8: DTMF/Tones Mode - Reserved, set to 0

Tx Mode Register b7-5: DTMF Twist (DTMF mode)
These 3 bits allow for adjustment of the DTMF twist to compensate for the frequency response of different external circuits. The device varies the twist by making changes to the upper tone group levels. Note that the twist cannot be adjusted mid-tone.

b7	b6	b5	
0	0	0	+2.0dB twist – normal setting when external response is flat
0	0	1	+1.0dB twist
0	1	0	+1.5dB twist
0	1	1	+2.5dB twist
1	0	0	+3.0dB twist
1	0	1	+3.5dB twist
1	1	0	+4.0dB twist
1	1	1	+4.5dB twist – do not use in conjunction with the 0dB Tx level setting

Tx Mode Register b4-0: DTMF/Tones mode
When DTMF/Tones transmit mode is selected (Tx Mode Register b15-12 = 0001), bits 4-0 select a DTMF signal or a fixed tone or one of four programmed tones or tone pairs for transmission.

b4 = 0: Tx fixed tone or programmed tone pair

b3	b2	b1	b0	Tone frequency (Hz)	
0	0	0	0	No tone	
0	0	0	1	697	
0	0	1	0	770	
0	0	1	1	852	
0	1	0	0	941	
0	1	0	1	1209	
0	1	1	0	1336	
0	1	1	1	1477	
1	0	0	0	1633	
1	0	0	1	1300	(Calling tone)
1	0	1	0	2100	(Answer tone)
1	0	1	1	2225	(Answer tone)
1	1	0	0	Tone pair TA	Programmed Tx tone or tone pair, see 6.10
1	1	0	1	Tone pair TB	“
1	1	1	0	Tone pair TC	“
1	1	1	1	Tone pair TD	“

b4 = 1: Tx DTMF

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

6.4 Receive Mode Register

Receive Mode Register: 16-bit write-only. C-BUS address $E2

This register controls the CMX869A receive signal type and level.

All bits of this register are cleared to 0 by a General Reset command or when b7 (Reset) of the General Control Register is 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Rx mode = modem				Rx level			Equaliser / De srambler			Start-stop/Synch			No. of bits and parity		
	Rx mode = Tones detect				Rx level			0	0	0	0	0	0	DTMF/Tones		
	Rx mode = Disabled				0	0	0	0	0	0	0	0	0	0	0	0

Rx Mode Register b15-12: Rx mode

These 4 bits select the receive operating mode.

b15	b14	b13	b12		
1	1	1	1	V.22, V.22 bis, V.32, V.32 bis	QAM AUTO modem
1	1	1	0	Reserved, do not use	
1	1	0	1	V.22 bis 2400	High band (Calling modem)
1	1	0	0	V.22bis 2400	Low band (Answering modem)
1	0	1	1	V.22 1200	High band (Calling modem)
1	0	1	0	V.22 1200	Low band (Answer modem)
1	0	0	1	V.21 300 bps FSK	High band (Calling modem)
1	0	0	0	"	Low band (Answering modem)
0	1	1	1	Bell 103 300 bps FSK	High band (Calling modem)
0	1	1	0	"	Low band (Answering modem)
0	1	0	1	V.23 FSK	1200 bps
0	1	0	0	"	75 bps
0	0	1	1	Bell 202 FSK	1200 bps
0	0	1	0	"	150 bps
0	0	0	1	DTMF, Programmed tone pair, Answer Tone, Call Progress detect	
0	0	0	0	Receiver disabled	

Rx Mode Register b11-9: Rx level

These three bits set the internal gain of the Rx Gain Control block.

b11	b10	b9	
1	1	1	0dB
1	1	0	-1.5dB
1	0	1	-3.0dB
1	0	0	-4.5dB
0	1	1	-6.0dB
0	1	0	-7.5dB
0	0	1	-9.0dB
0	0	0	-10.5dB

Rx Mode Register b8: Rx Auto-equalise (DPSK/QAM manual modem modes)
This bit controls the operation of the receive DPSK/QAM auto-equaliser. Set to 0 in FSK modes. Set to 1 in 2400bps QAM mode. No effect in Auto Modem modes.

b8 = 1	Enable auto-equaliser
b8 = 0	DPSK mode: Auto-equaliser disabled QAM mode : Auto-equaliser settings frozen

Rx Mode Register b7-6: Rx Scrambler (DPSK/QAM manual modem modes)
These 2 bits control the operation of the Rx descrambler used in QAM and DPSK modes. Set both bits to 0 in FSK modes. No effect in Auto Modem modes.

b7	b6	
1	1	Descrambler enabled, 64 ones detect circuit enabled (normal use)
1	0	Descrambler enabled, 64 ones detect circuit disabled
0	1	Reserved, do not use
0	0	Descrambler disabled

Rx Mode Register b5-3: Rx Modem Data format
These three bits select the Rx modem USART operating mode. The 1% and 2.3% overspeed options apply to QAM modes only.

b5	b4	b3	
1	1	1	Rx Special modes
1	1	0	Rx Start-stop mode, no overspeed
1	0	1	Rx Start-stop mode, +1% overspeed (1 in 8 missing Stop bits allowed)
1	0	0	Rx Start-stop mode, +2.3% overspeed (1 in 4 missing Stop bits allowed)
0	1	1	Reserved, do not use
0	1	0	Reserved, do not use
0	0	1	Reserved, do not use
0	0	0	Rx USART function disabled

Rx Mode Register b2-0: Rx Modem Data bits and Parity (Start-Stop modes)
In Start-stop mode these three bits select the number of data bits (plus any parity bit) in each received character.

b2	b1	b0	
1	1	1	8 data bits + parity
1	1	0	8 data bits
1	0	1	7 data bits + parity
1	0	0	7 data bits
0	1	1	6 data bits + parity
0	1	0	6 data bits
0	0	1	5 data bits + parity
0	0	0	5 data bits

Rx Mode Register b2-0: Rx Modem Data bits and Parity (Special modes)

When b5-3 = 111 bits 2-0 select special receive modes as below:

b2	b1	b0	
1	1	1	Synchronous, received bits transferred directly to Rx Data Register
1	1	0	HDLC mode
1	0	1	Reserved, do not use.
1	0	0	Reserved, do not use.
0	1	1	Reserved, do not use.
0	1	0	Reserved, do not use.
0	0	1	Reserved, do not use.
0	0	0	Reserved, do not use.

Rx Mode Register b2-0: Tones Detect mode

In Tones Detect Mode (Rx Mode Register b15-12 = 0001) b8-3 should be set to 000000.
Bits 2-0 select the detector type.

b2	b1	b0	
1	1	1	Reserved, do not use.
1	1	0	Reserved, do not use.
1	0	1	Reserved, do not use.
1	0	0	Programmable Tone Pair Detect
0	1	1	Call Progress Detect
0	1	0	2100, 2225Hz Answer Tone Detect
0	0	1	DTMF Detect
0	0	0	Disabled

6.5 QAM AUTO Modem Command Register

QAM AUTO Modem Command Register: 16-bit write-only. C-BUS address $EA

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	0	0	0	0	0	0	0	0	0	0	Command					
														Protocol/Bit Rate		

The V.22, V.22 bis, V.32, V.32 bis QAM AUTO modem is controlled by writing the commands listed below to this register. B15-6 should all be cleared to 0. These commands will not take effect unless both Tx and Rx Mode Registers have both been set to QAM AUTO modem mode. This register should only be written to when b13 (Programming Flag bit) of the Status Register is 1.

b5	b4	b3	b2	b1	b0	**Command**
0	0	0	0	0	0	Stop modem
F	0	1	Max bitrate			Initiate retrain
F	1	0	Max bitrate			Start automodem in calling mode
F	1	1	Max bitrate			Start automodem in answer mode
1	0	0	Max bitrate			Initiate rate re-negotiation

F is the fast training flag bit:

In V.22 or V.22 bis AUTO modes: If F is set to 1 in a 'start automodem in answer mode' command the 2100Hz answer tone will not be transmitted. The F bit has no effect in other commands.

In V.32 or V.32 bis AUTO modes: If F is set to 1 a faster but less accurate echo cancellation training algorithm is used.

The 'Max bitrate' field defines the maximum bitrate that will be allowed by the modem during rate negotiations.

Bit:	**Max bitrate** b2	b1	b0	**bps**	**Protocol**
	1	1	1	14400	V.32 bis
	1	1	0	12000	V.32 bis
	1	0	1	9600	V.32 / V.32 bis (with Trellis coding)
	1	0	0	9600	V.32 (no Trellis coding)
	0	1	1	7200	V.32 bis
	0	1	0	4800	V.32 / V.32 bis
	0	0	1	2400	V.22 bis
	0	0	0	1200	V.22 / V.22 bis

For most applications a connection can be established by ensuring that the Tx and Rx Mode registers have been set to QAM AUTO modem mode and that the Status Register b13 = 1 then writing a 'Start automodem (calling or answer mode)' command with the Max bitrate field set to 14400bps. The CMX869A will automatically attempt to execute the entire start-up procedure as described in V.32 bis, including the V.25 automatic answering sequence, receiver training and rate negotiation. Significant events occurring during this process will be reported in the QAM AUTO Modem Status Register.

When a data connection has been established b3-0 of the QAM AUTO Modem Status Register will show a value of between 1000 and 1111, indicating the negotiated bit rate. Following a sucessful connection, the SNR value should be monitored by the host to determine if a re-train or rate re-negotiation is required, should the line conditions deteriorate.

The CMX869A will automatically respond to V.32/V.32 bis retrain and rate re-negotiation requests from the distant modem; alternatively the 'Initiate retrain' and 'Initiate rate re-negotiation' commands can be used to initiate such requests. In both cases the progress of the retrain or rate re-negotiation will be reported in the QAM Modem Status Register. If the rate re-negotiation is unsuccessful with the maximum bit rate set to 4800 baud or above, re-initiate the rate re-negotiation with the maximum bit rate set to 2400 baud (V.22bis) or less.

6.6 Tx Data Register

Tx Data Register: 8 or 16-bit write-only. C-BUS addresses $E3 and $E4

This register may be set to operate in 8 or 16-bit mode by b10 of the General Control Register. This setting should not be changed once data transmission has started.

1-character mode (General Control Register b10 = 0). C-Bus addresses $E3 and $E4

Bit:	7	6	5	4	3	2	1	0
	Byte to be transmitted							

2-character mode (General Control Register b10 = 1). C-Bus address $E3 only

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	First byte to be transmitted								Second byte to be transmitted							

This register should only be written to when the Tx Data Ready bit of the Status Register is set to 1.

In Synchronous Tx data mode all 8 bits of a byte are transmitted, bit 0 of each byte being transmitted first. In Tx Start-Stop modes the specified number of data bits will be taken from the byte in the Tx Data Register (b0 of the byte first). A Start bit, a Parity bit (if required) and Stop bit(s) will be added automatically.

C-BUS address $E3 should normally be used, $E4 has special functions depending on the setting of b10 of the General Control Register:

If General Control Register b10 = 0 (1-character mode) then address $E4 is used to implement the V.14 overspeed transmission requirement in Start-Stop mode, see section 5.1.

If General Control Register b10 = 1 (2-character mode) then a single character can be transmitted, say at the end of a message, by writing it as a single byte to address $E4. V.14 operation is not supported in this mode.

6.7 Rx Data Register

Rx Data Register: 8 or 16-bit read-only. C-BUS address $E5

This register may be set to operate in 8 or 16-bit mode by b10 of the General Control Register (note: this setting is only actioned following a reset or power-on).

1-character mode (General Control Register b10 = 0).

Bit:	7	6	5	4	3	2	1	0
	Received byte/character							

2-character mode (General Control Register b10 = 1).

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	First received byte/character								Second received byte/character							

In Synchronous and HDLC Rx data modes each byte contains 8 received data bits, b0 of the byte holding the earliest received bit, b7 the latest.

In Start-Stop modes each byte contains the specified number of data bits from a received character, b0 of the byte holding the first received bit. Unused bits are set to 0.

In HDLC mode, the FCS will be output in this register following the last received data character.

6.8 Status Register

Status Register: 16-bit read-only. C-BUS address $E6

Bits 13-0 of this register are cleared to 0 by a General Reset command or when b7 (Reset) of the General Control Register is 1, or while b8 (Power-Up) of the General Control Register is 0.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRQ	RD	PF	TxD	TxU	See below for uses of these bits										

The meanings of the Status Register bits 10-0 depend on the receive mode.

Status Register bits 15-11: All modes		**IRQ Mask bit**
b15	IRQ.	b6
b14	Set to 1 on Ring Detect	b5
b13	Programming Flag bit. See 6.10	b4
b12	Set to 1 on Tx data ready. Cleared by write to Tx Data Register	b3
b11	Set to 1 on Tx data underflow. Cleared by write to Tx Data Register	b3

Status Register bits 10-0: Rx Tones Detect modes		IRQ Mask bit
b10	Set to 1 when energy is detected in Call Progress band or when both programmable tones are detected	b2
b9	0	b1
b8	0	b1
b7	Set to 1 when 2100Hz answer tone or when the second programmable tone is detected	b1
b6	Set to 1 when 2225Hz answer tone or when the first programmable tone is detected	b0
b5	Set to 1 when DTMF code is detected	b0
b4	0	-
b3	Rx DTMF code b3, see table following	-
b2	Rx DTMF code b2	-
b1	Rx DTMF code b1	-
b0	Rx DTMF code b0	-

Status Register bits 10-7: Rx FSK Modem modes		IRQ Mask bit
b10	1 while energy is detected in Rx modem signal band	b2
b9	1 while '1010..' or '11001100..' S1 pattern is detected	b1
b8	See following table	b1
b7	See following table	b1

b8	b7	Descrambler disabled	Descrambler enabled (DPSK/QAM MANUAL modes only)
1	1	-	Continuous scrambled 1s (see note)
1	0	Continuous unscrambled 0s	Continuous scrambled 0s
0	1	Continuous unscrambled 1s	Continuous unscrambled 1s
0	0	-	-

Status Register bits 10-7: QAM AUTO MODEM modes		IRQ Mask bit
b10	0	b2
b9	Set to 1 by modem event. Cleared by read of QAM modem Status Register	b1
b8	Set to 1 when V.14 'break' signal detected in Start-Stop mode	b1
b7	0	b1

Status Register bits 6-0: All Rx Modem modes		IRQ Mask bit
b6	Set to 1 on Rx data ready. Cleared by read from Rx Data Register	b0
b5	Set to 1 on Rx data overflow. Cleared by read from Rx Data Register	b0
b4	Set to 1 on Rx UART framing error or HDLC FCS error	-
b3	Start-Stop mode: set to 1 if Rx character has even parity (first character if in 2-character mode) HDLC mode: set to 1 when last byte (FCS) of HDLC packet is received	-
b2	Start-Stop mode: 1 if second Rx character has even parity (2-character mode)	-
b1	Set to 1 if Rx Data Register contains 2 characters (2-character mode)	-
b0	FSK frequency demodulator output (0 in QAM modes)	-

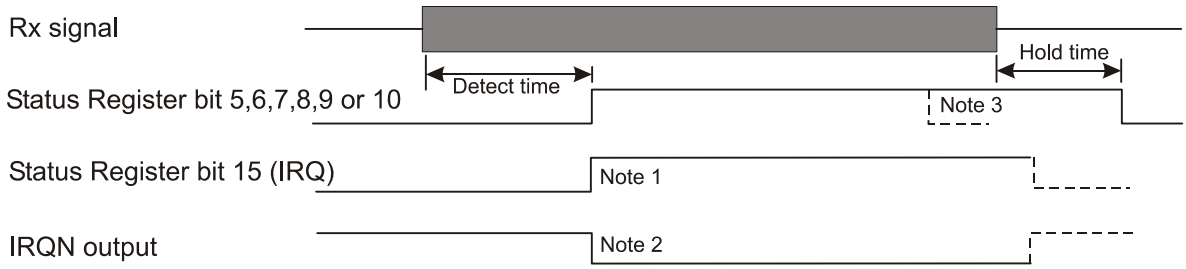
Notes:

When the descrambler is enabled then detection of continuous unscrambled 1s will inhibit the continuous scrambled 1s detector.

The IRQ Mask Bit column shows the corresponding IRQ Mask bits in the General Control Register. A 0 to 1 transition on any of the Status Register bits 14-5 will cause the IRQ bit 15 to be set to 1 if the corresponding IRQ Mask bit is 1. The IRQ bit is cleared by a read of the Status Register or a General Reset command or by setting b7 or b8 of the General Control Register to 1.

The IRQN output pin will be pulled low (to VSS) when the IRQ bit of the Status Register and the IRQNEN bit (b6) of the General Control Register are both set to 1.

The operation of the FSK data demodulator and pattern detector circuits within the CMX869A do NOT depend on the state of the Rx energy detect function.



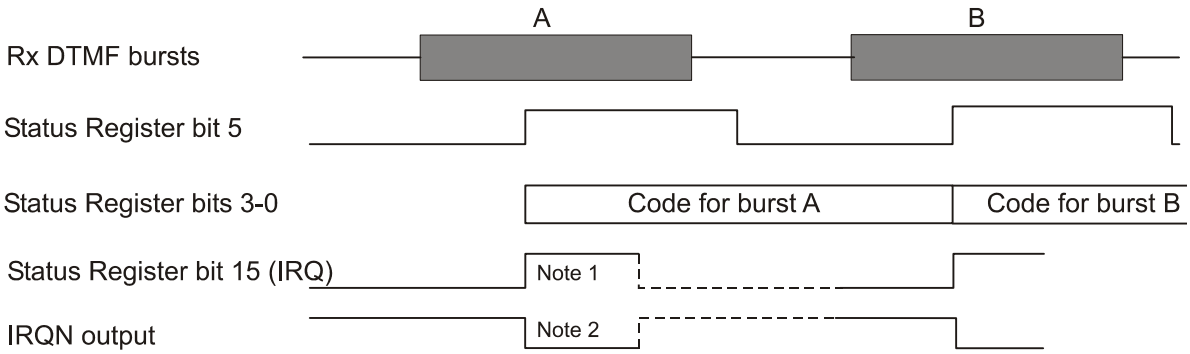
Notes:
1. IRQ will go high only if appropriate IRQ Mask bit in General Control Register is set to 1. The IRQ bit is cleared to 0 by a read of the Status Register.
2. IRQN output will go low when IRQ bit goes high, if IRQNEN bit of General Control Register is set to 1.
3. In Rx Modem modes Status Register bits 5 and 6 are set to 1 by an Rx Data Ready or Rx Data Overflow event and cleared to 0 by a read of the Rx Data Register.

Figure 9a Operation of Status Register bits 5-10

Changes to Status Register bits caused by a change of Tx or Rx operating mode can take up to 150μs to take effect.

The Ring Detect bit (b14) continues to operate in Powersave mode or when the Reset bit (b7) of the General Control Register is 1. The Ring Detect bit follows the inverted state of the RDN input pin. An interrupt is only generated as a result of a negative transition on the RDN pin, if General Control Register bits 5 and 6 are set to 1.

In Rx FSK modem modes bit 0 will show the output of the frequency demodulator, updated at 8 times the nominal data rate.



Notes:
1. IRQ will go high only if the IRQ Mask bit 0 in the General Control Register is set to 1. The IRQ bit is cleared to 0 by a read of the Status Register.
2. IRQN output will go low when IRQ bit goes high, if IRQNEN bit of General Control Register is set to 1.

Figure 9b Operation of Status Register in DTMF Rx Mode

b3	b2	b1	b0	Low frequency (Hz)	High frequency (Hz)	Keypad symbol
0	0	0	0	941	1633	D
0	0	0	1	697	1209	1
0	0	1	0	697	1336	2
0	0	1	1	697	1477	3
0	1	0	0	770	1209	4
0	1	0	1	770	1336	5
0	1	1	0	770	1477	6
0	1	1	1	852	1209	7
1	0	0	0	852	1336	8
1	0	0	1	852	1477	9
1	0	1	0	941	1336	0
1	0	1	1	941	1209	*
1	1	0	0	941	1477	#
1	1	0	1	697	1633	A
1	1	1	0	770	1633	B
1	1	1	1	852	1633	C

Received DTMF Code: b3-0 of Status Register

6.9 QAM AUTO Modem Status Register

QAM AUTO Modem Status Register: 16-bit read-only. C-BUS address $EB
This register should only be read from when b13 (Programming Flag bit) of the Status Register is 1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Messages						0	0	0	SNR			Mode			

QAM AUTO Modem Status Register b15-10: Messages

b15	b14	b13	b12	b11	b10	
1	1	1	Bit Rate			R5 received
1	1	0	Bit Rate			R4 received
1	0	1	Bit Rate			R3 received
1	0	0	Bit Rate			R2 received
0	1	1	Bit Rate			R1 received
0	1	0	1	1	1	Rate negotiation request detected
0	1	0	1	1	0	Retrain request detected
0	1	0	1	0	1	Emergency retrain started
0	1	0	1	0	0	Carrier lost
0	1	0	0	1	1	V.32 preamble detected
0	1	0	0	1	0	S1 detected
0	1	0	0	0	1	SB1 detected
0	1	0	0	0	0	USB1 detected
0	0	1	1	1	1	2100Hz detected
Other combinations of b15-10						unused

Bit Rate field of Messages (see above)

b12	b11	b10		
1	1	1	14400	V.32 bis
1	1	0	12000	V.32 bis
1	0	1	9600	V.32 / V.32 bis (with Trellis coding)
1	0	0	9600	V.32 (no Trellis coding)
0	1	1	7200	V.32 bis
0	1	0	4800	V.32 / V.32 bis
0	0	1	2400	V.22 bis
0	0	0	1200	V.22 / V.22 bis

QAM AUTO Modem Status Register b9-7: Unused (000)

QAM AUTO Modem Status Register b6-4: Signal to Noise

b6	b5	b4	
1	1	1	Very good; could increase rate or retrain
1	1	0	Good
1	0	1	Normal
1	0	0	Poor
0	1	1	Bad; receiver will have a high error rate
0	1	0	Really bad; should decrease data rate or retrain
0	0	1	Unused
0	0	0	SNR not yet determined

QAM AUTO Modem Status Register b3-0: Operating Mode

b3	b2	b1	b0		
1	1	1	1	14400 bps	V.32 bis
1	1	1	0	12000 bps	V.32 bis
1	1	0	1	9600 bps	V.32 / V.32 bis (with Trellis coding)
1	1	0	0	9600 bps	V.32 (no Trellis coding)
1	0	1	1	7200 bps	V.32 bis
1	0	1	0	4800 bps	V.32 / V.32 bis
1	0	0	1	2400 bps	V.22 bis
1	0	0	0	1200 bps	V.22 / V.22 bis
0	1	1	1	Unused	
0	1	1	0	Unused	
0	1	0	1	Unused	
0	1	0	0	Training / Rate negotiation	
0	0	1	1	Transmitting 2100Hz answer tone	
0	0	1	0	Tx silence, Rx idle	
0	0	0	1	Tx idle, Rx waiting	
0	0	0	0	Idle	

An update to the Messages status (b15 – b10) or any change in SNR or Mode status (b6 – b0) will cause b9 of the main Status Register to be set to 1.

6.10 Programming Register

Programming Register : 16-bit write-only. C-BUS address $E8
This register is used to program the transmit and receive programmed tone pairs by writing appropriate values to RAM locations within the CMX869A. Note that these RAM locations are cleared by Powersave or Reset.

The Programming Register should only be written to when the Programming Flag bit (b13) of the Status Register is 1. The act of writing to the Programming Register clears the Programming Flag bit. When the programming action has been completed (normally within 150μs) the CMX869A will set the bit back to 1.

When programming Transmit or Receive Tone Pairs, do not change the Transmit or Receive Mode Registers until programming is complete and the Programming Flag bit has returned to 1.

Transmit Tone Pair Programming
4 transmit tone pairs (TA to TD) can be programmed.

The frequency (max 3.4kHz) and level must be entered for each tone to be used.

Single tones are programmed by setting both level and frequency values to zero for one of the pair.

Programming is done by writing a sequence of seventeen 16-bit words to the Programming Register. The first word should be 32768 (8000 hex), the following 16-bit words set the frequencies and levels and are in the range 0 to 16383 (0-3FFF hex)

Word	Tone Pair	Value written
1		32768
2	TA	Tone 1 frequency
3	TA	Tone 1 level
4	TA	Tone 2 frequency
5	TA	Tone 2 level
6	TB	Tone 1 frequency
7	TB	Tone 1 level
- - -	- - -	- - - - - - - - - -
- - -	- - -	- - - - - - - - - -
16	TD	Tone 2 frequency
17	TD	Tone 2 level

The Frequency values to be entered are calculated from the formula:

Value to be entered = desired frequency (Hz) * 3.414

i.e. for 1kHz the value to be entered is 3414 (or 0D56 in Hex).

The Level values to be entered are calculated from the formula:

Value to be entered = desired Vrms * 93780 / AV_{DD}

i.e. for 0.5Vrms at AV_{DD} = 3.3V, the value to be entered is 14209 (3781 in Hex)

Programming a notone pair is done by writing zero to all four tone pair words. On power-up or after a reset, the tone pairs TA-TC are set to notone, and TD is set to generate 2130Hz + 2750Hz at approximately –18dBm (100mVrms) each. Unprogrammed tone pairs retain their previous values.

Allowance should be made for the transmit signal filtering in the CMX869A which attenuates the output signal for frequencies above 2kHz, by 0.25dB at 2.5kHz, by 1dB at 3kHz, and by 2.2dB at 3.4kHz.

Receive Tone Pair Programming

The Programmable Tone Pair Detector is implemented as shown in Figure 10a. The filters are 4th order IIR sections. The frequency detectors measure the time taken for a programmable number of complete input signal cycles and compare this time against programmable upper and lower limits.

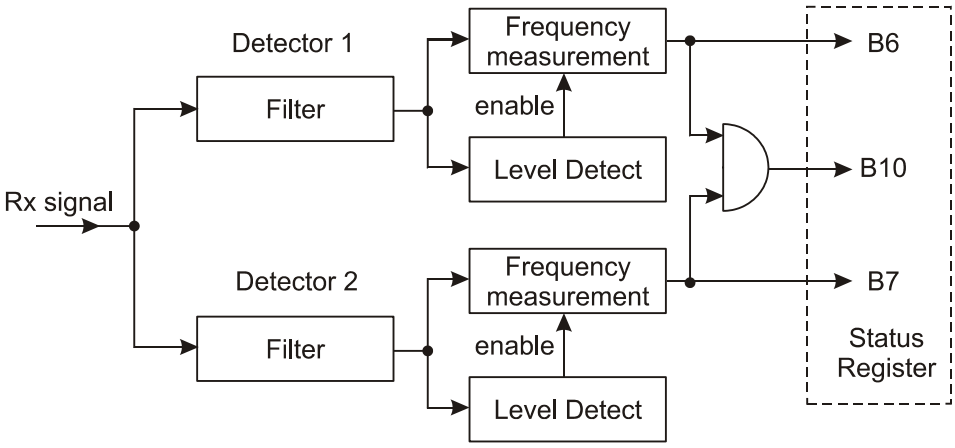


Figure 10a Programmable Tone Pair Detector

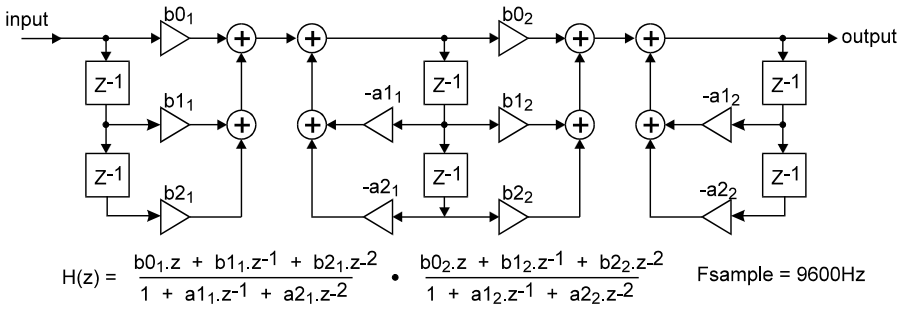


Figure 10b Filter Implementation

Programming is done by writing a sequence of twenty-seven 16-bit words to the Programming Register. The first word should be 32769 (8001 hex), the following twenty-six 16-bit words set the frequencies and levels and are in the range 0 to 32767 (0000-7FFF hex).

Word	Value written	Word	Value written
1	32769		
2	Filter #1 coefficient $b2_1$	15	Filter #2 coefficient $b2_1$
3	Filter #1 coefficient $b1_1$	16	Filter #2 coefficient $b1_1$
4	Filter #1 coefficient $b0_1$	17	Filter #2 coefficient $b0_1$
5	Filter #1 coefficient $a2_1$	18	Filter #2 coefficient $a2_1$
6	Filter #1 coefficient $a1_1$	19	Filter #2 coefficient $a1_1$
7	Filter #1 coefficient $b2_2$	20	Filter #2 coefficient $b2_2$
8	Filter #1 coefficient $b1_2$	21	Filter #2 coefficient $b1_2$
9	Filter #1 coefficient $b0_2$	22	Filter #2 coefficient $b0_2$
10	Filter #1 coefficient $a2_2$	23	Filter #2 coefficient $a2_2$
11	Filter #1 coefficient $a1_2$	24	Filter #2 coefficient $a1_2$
12	Freq measurement #1 ncycles	25	Freq measurement #2 ncycles
13	Freq measurement #1 mintime	26	Freq measurement #2 mintime
14	Freq measurement #1 maxtime	27	Freq measurement #2 maxtime

The coefficients are entered as 15-bit signed (two's complement) integer values (the most significant bit of the 16-bit word entered should be zero) calculated as 8192 * coefficient value from the user's filter design program (i.e. this allows for filter design values of -1.9999 to +1.9999).

The design of the IIR filters should make allowance for the fixed receive signal filtering in the CMX869A which has a low pass characteristic above 1.5kHz, of 0.4dB at 2kHz, 1.2dB at 2.5kHz, 2.6dB at 3kHz and 4.1dB at 3.4kHz.

'ncycles' is the number of signal cycles for the frequency measurement.

'mintime' is the smallest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'mintime' = 9600 * ncycles / high frequency limit

'maxtime' is the highest acceptable time for ncycles of the input signal expressed as the number of 9.6kHz timer clocks. i.e. 'maxtime' = 9600 * ncycles / low frequency limit

The level detectors include hysteresis. The threshold levels - measured at the 2 or 4-wire line with unity gain filters, using the line interface circuits described in section 4.3, 1.0 dB line coupling transformer loss and with the Rx Gain Control block set to 0dB - are nominally:

'Off' to 'On'	-42.0dBm
'On' to 'Off'	-44.5dBm

Note that if any changes are made to the programmed values while the CMX869A is running in Programmed Tone Detect mode they will not take effect until the CMX869A is next switched into Programmed Tone Detect mode.

On power-up or after a reset, the programmable tone pair detector is set to act as a simple 2130Hz + 2750Hz detector.

7. Application Notes

Simple Auto-modem connect sequence

This sequence will set up a V32bis Automodem call between two directly connected CMX869A's (ie: NOT routing through a telephone line. This is used to demonstrate the Automodem capability).

	CBUS address	value(dec) calling modem	value(hex) calling modem	value(dec) answering modem	value(hex) answering modem	
wr	01					reset
wr	E0	320	140	320	140	power up relevant sections
wr	E1	61462	F016	61462	F016	set tx mode and level to QAM, -10dB
wr	E3	61494	F036	61494	F036	set rx mode and level to QAM, -10dB
		offhook		offhook		If needed
wr	EA	23	17	31	1F	Start auto modem mode
		Connect in progress				...wait a bit
rd	EB?	48239	BC6F	19460	4C04	read back the QAM status
		Now send some data				
wr	E4	66	42	66	42	send ASCII char 'B'
rd	E5?	66	42	66	42	should receive ASCII char 'B'

V22bis Manual connect sequence

See Application Notes on the CML website.

8. Performance Specification

8.1 Electrical Performance

8.1.1 Absolute Maximum Ratings

Exceeding these maximum ratings can result in damage to the device.

	Min.	Max.	Units
Supply (AV_{DD} - AV_{SS}) or (DV_{DD} - DV_{SS})	-0.3	+4.0	V
Voltage on any pin (except V_{DEC}) to AV_{SS} or DV_{SS}	-0.3	V_{DD} + 0.3	V
Voltage between AV_{SS} and DV_{SS}	-50	+50	mV
Voltage between AV_{DD} and DV_{DD}	-300	+300	mV
Current into or out of AV_{SS}, DV_{SS}, AV_{DD} or DV_{DD} pins	-50	+50	mA
Current into RDRVN pin (RDRVN pin low)		+50	mA
Current into or out of any other pin	-20	+20	mA

D2 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		1000	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

E2 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		400	mW
... Derating		5.3	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

P4 Package	**Min.**	**Max.**	**Units**
Total Allowable Power Dissipation at Tamb = 25°C		1000	mW
... Derating		13	mW/°C
Storage Temperature	-55	+125	°C
Operating Temperature	-40	+85	°C

8.1.2 Operating Limits

Correct operation of the device outside these limits is not implied.

	Notes	**Min.**	**Max.**	**Units**
Supply (AV_{DD} - AV_{SS}) and (DV_{DD} - DV_{SS})		3.0	3.6	V
Supply rise time (10% to 90%)			25	ms
Operating Temperature		-40	+85	°C

8.1.3 Operating Characteristics

For the following conditions unless otherwise specified:
V_{DD} = AV_{DD} = DV_{DD} = 3.0V to 3.6V at Tamb = -40 to +85°C; V_{SS} = AV_{SS} = DV_{SS};
Xtal Frequency = 6.144MHz ± 0.005% (50ppm);
0dBm corresponds to 775mVrms. General Control Register bit 14 = 0 (High Rx Gain turned off).

DC Parameters	Notes	Min.	Typ.	Max.	Units
I_{DD} (Powersave mode)	1, 2	-	20	100	µA
(Reset but not powersave)	1, 3	-	3.0	5.0	mA
(Running, AV_{DD} = DV_{DD} = 3.3V)	1	-	8.6	13.0	mA
Logic '1' Input Level	4	70%	-	-	DV_{DD}
Logic '0' Input Level	4	-	-	30%	DV_{DD}
Logic Input Leakage Current (Vin = 0 to DV_{DD}), (excluding XTAL/CLOCK input)		-1.0	-	+1.0	µA
Output Logic '1' Level (I_{OH} = 0.6 mA)		80%	-	-	V_{DD}
Output Logic '0' Level (I_{OL} = -1.0 mA)		-	-	+0.4	V
IRQN O/P 'Off' State Current (Vout = V_{DD})		-1.0	-	+1.0	µA
RDN pin Schmitt trigger input high-going threshold (Vthi) (see Figure 11)		0.56 V_{DD}	-	0.56 V_{DD} +0.6	V
RDN pin Schmitt trigger input low-going threshold (Vtlo) (see Figure 11)		0.44 V_{DD} -0.6	-	0.44 V_{DD}	V
RDRVN 'ON' resistance to DV_{SS} (DV_{DD}= 3.3V)		-	50	70	Ω
RDRVN 'OFF' resistance to DV_{DD} (DV_{DD}= 3.3V)		-	1170	3000	Ω

Notes:
1. At 25°C, not including any current drawn from the CMX869A pins by external circuitry other than X1, C5 and C6.
2. All logic inputs at DV_{SS} except CSN input which is at DV_{DD}.
3. General Control Register b8 and b7 both set to 1.
4. Excluding RDN pin.

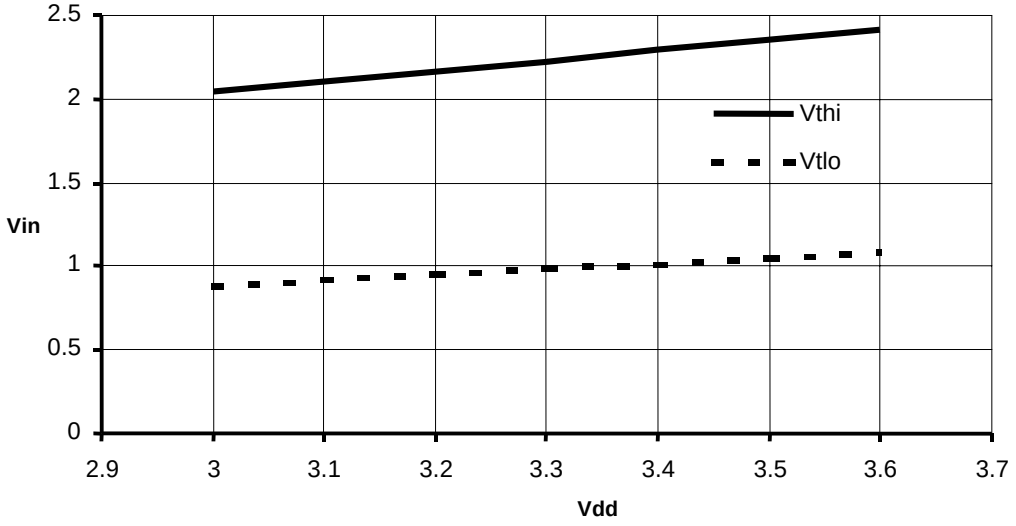


Figure 11 Typical Schmitt Trigger Input Voltage Thresholds vs. V_{DD}

XTAL/CLOCK Input (timings for an external clock input)	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
'High' Pulse Width		60	-	-	ns
'Low' Pulse Width		60	-	-	ns

Transmit Output Level	**Notes**	**Min.**	**Typ.**	**Max.**	**Units**
Modem and Single Tone modes	5	-1.5	-0.5	0.5	dBm
DTMF mode, Low Group tones	5	0.5	1.5	2.5	dBm
DTMF: level of High Group tones wrt Low Group	5	+1.0	+2.0	+3.0	dB
Tx output buffer gain control accuracy	5	-0.25	-	+0.25	dB
Tx output impedance (TXA or TXAN)			6.0		ohm

Notes: 5. Measured between TXA and TXAN pins with Tx Level Control gain set to 0dB, 1.2kΩ load between TXA and TXAN, at AV_{DD} = 3.3V (levels are proportional to AV_{DD} - see section 4.3). Level measurements for all modem modes are performed with random transmitted data and without any guard tone. 0dBm = 775mVrms. DTMF twist set to +2.0dB.

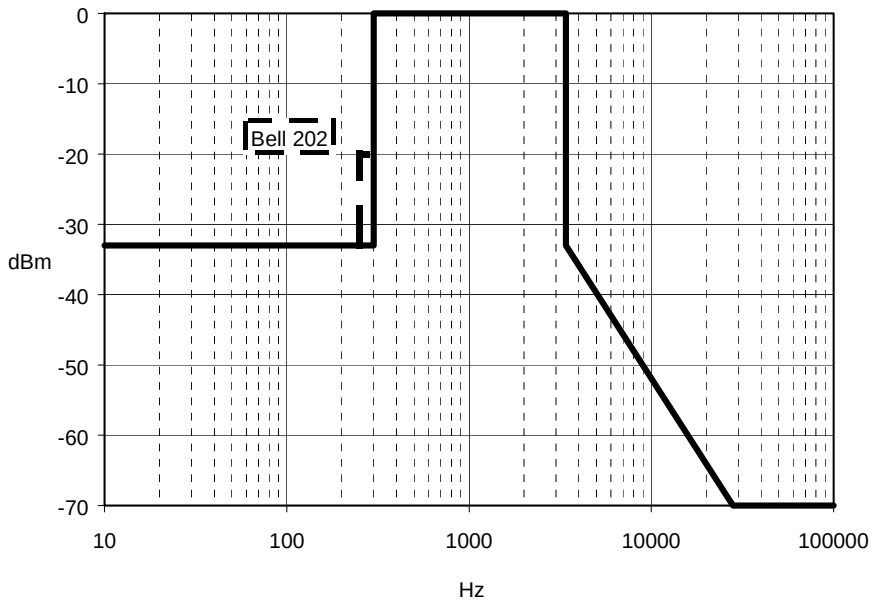


Figure 12 Maximum Out of Band Tx Line Energy Limits (see note 6)

Notes: 6. Measured on the 2 or 4-wire line using the line interface circuits described in section 4.3 with the Tx line signal level set to -10dBm for any modem mode or single tones, -6dBm and -8dBm for DTMF tones. Excludes any distortion due to external components such as the line coupling transformer.

Rx Modem Energy Detector (FSK modes)	Notes	Min.	Typ.	Max.	Units
Detect threshold (‘Off’ to ‘On)	7, 8	-	-	-43.0	dBm
Undetect threshold (‘On’ to ‘Off’)	7, 8	-48.0	-	-	dBm
Hysteresis	7, 8	2.0	-	-	dB
Detect (‘Off’ to ‘On’) response time					
300 and 1200 baud FSK modes	7, 8	8.0	-	30.0	ms
150 and 75 baud FSK modes	7, 8	16.0	-	60.0	ms
Undetect (‘On’ to ‘Off’) response time					
300 and 1200 baud FSK modes	7, 8	10.0	-	40.0	ms
150 and 75 baud FSK modes	7, 8	20.0	-	80.0	ms

Rx Answer Tone Detectors	Notes	Min.	Typ.	Max.	Units
Detect threshold (‘Off’ to ‘On)	7,9	-	-	-43.0	dBm
Undetect threshold (‘On’ to ‘Off’)	7,9	-48.0	-	-	dBm
Detect (‘Off’ to ‘On’) response time	7,9	30.0	33.0	45.0	ms
Undetect (‘On’ to ‘Off’) response time	7,9	7.0	18.0	25.0	ms
2100Hz detector					
‘Will detect’ frequency		2050	-	2160	Hz
‘Will not detect’ frequency		-	-	2000	Hz
2225Hz detector					
‘Will detect’ frequency		2160	-	2285	Hz
‘Will not detect’ frequency		2335	-	-	Hz

Rx Call Progress Energy Detector	Notes	Min.	Typ.	Max.	Units
Bandwidth (-3dB points) See Figure 6		275	-	665	Hz
Detect threshold (‘Off’ to ‘On)	7,10	-	-	-37.0	dBm
Undetect threshold (‘On’ to ‘Off’)	7,10	-42.0	-	-	dBm
Detect (‘Off’ to ‘On’) response time	7,10	30.0	36.0	45.0	ms
Undetect (‘On’ to ‘Off’) response time	7,10	6.0	8.0	50.0	ms

Notes: 7. Rx 2 or 4-wire line signal level with Rx Gain Control block set to 0dB and external components of section 4.3 set so that level at RXAFB pin is 3.6dB below the line signal level. Measured at AV_{DD} = 3.3V.

8. Thresholds and times measured with continuous binary ‘1’ for all FSK modes. Times measured with signal switched between off and -33dBm

9. ‘Typical’ value refers to 2100Hz or 2225Hz signal switched between off and -33dBm. Times measured wrt. received line signal.

10. ‘Typical’ values refers to 400Hz signal switched between off and -33dBm.

DTMF Decoder	Notes	Min.	Typ.	Max.	Unit
Valid input signal levels (each tone of composite signal)	7	-30.0	-	0.0	dBm
Not decode level (either tone of composite signal)	7	-	-	-36.0	dBm
Twist = High Tone/Low Tone		-11.0	-	16.0	dB
Frequency Detect Bandwidth	12	±1.8	-	-	%
Frequency Not Detect Bandwidth	12	-	-	±3.5	%
Max level of low frequency noise (i.e dial tone)					
Interfering signal frequency <= 550Hz	11	-	-	0.0	dB
Interfering signal frequency <= 450Hz	11	-	-	10.0	dB
Interfering signal frequency <= 200Hz	11	-	-	20.0	dB
Max. noise level wrt. signal	11,14	-	-	-10.0	dB
DTMF detect response time	13	-	-	40.0	ms
DTMF de-response time	13	-	-	30.0	ms
Status Register b5 high time		14.0	-	-	ms
'Will Detect' DTMF signal duration		40.0	-	-	ms
'Will Not Detect' DTMF signal duration		-	25.0	-	ms
Pause length detected		30.0	-	-	ms
Pause length ignored		-	-	15.0	ms

Notes:
11. Referenced to DTMF tone of lower amplitude
12. Under conditions of the Mitel CM7291 test tape
13. See figure 9b for timing information
14. Flat Gaussian Noise in 300-3400Hz band.

Receive Input Amplifier	Notes	Min.	Typ.	Max.	Units
Input impedance (at 100Hz)		10.0			Mohm
Open loop gain (at 100Hz)			10000		V/V
Rx Gain Control Block accuracy		-0.25		+0.25	dB

C-BUS Timings (See Figure 13)		Notes	Min.	Typ.	Max.	Units
t_{CSE}	CSN-Enable to Clock-High time		100	-	-	ns
t_{CSH}	Last Clock-High to CSN-High time		100	-	-	ns
t_{LOZ}	Clock-Low to Reply Output enable time		0.0	-	-	ns
t_{HIZ}	CSN-High to Reply Output 3-state time		-	-	1.0	µs
t_{CSOFF}	CSN-High Time between transactions		1.0	-	-	µs
t_{NXT}	Inter-Byte Time		200	-	-	ns
t_{CK}	Clock-Cycle time		200	-	-	ns
t_{CH}	Serial Clock-High time		100	-	-	ns
t_{CL}	Serial Clock-Low time		100	-	-	ns
t_{CDS}	Command Data Set-Up time		75.0	-	-	ns
t_{CDH}	Command Data Hold time		25.0	-	-	ns
t_{RDS}	Reply Data Set-Up time		50.0	-	-	ns
t_{RDH}	Reply Data Hold time		0.0	-	-	ns

Maximum 30pF load on each C-BUS interface line.

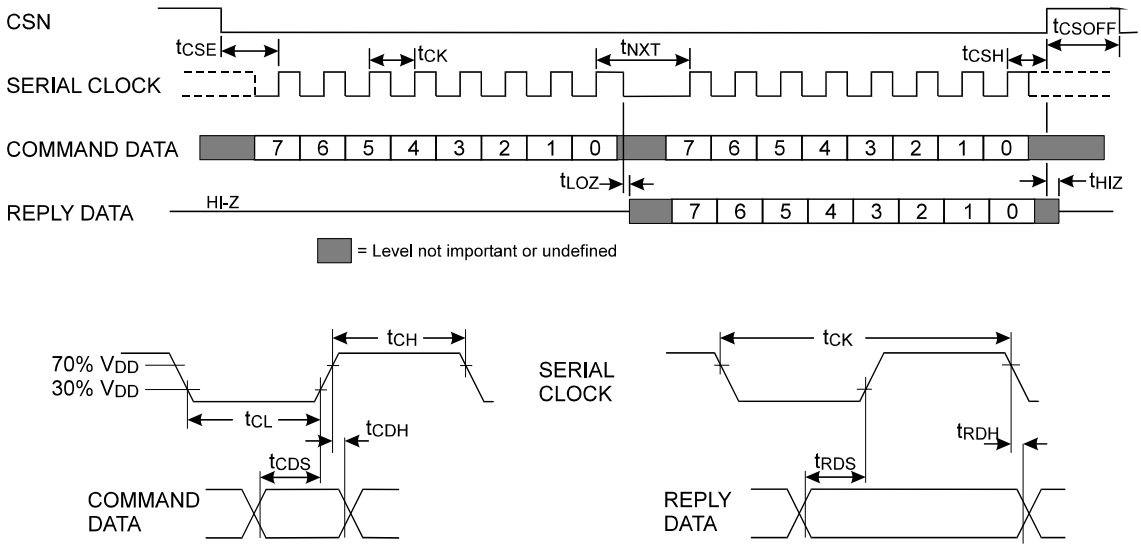
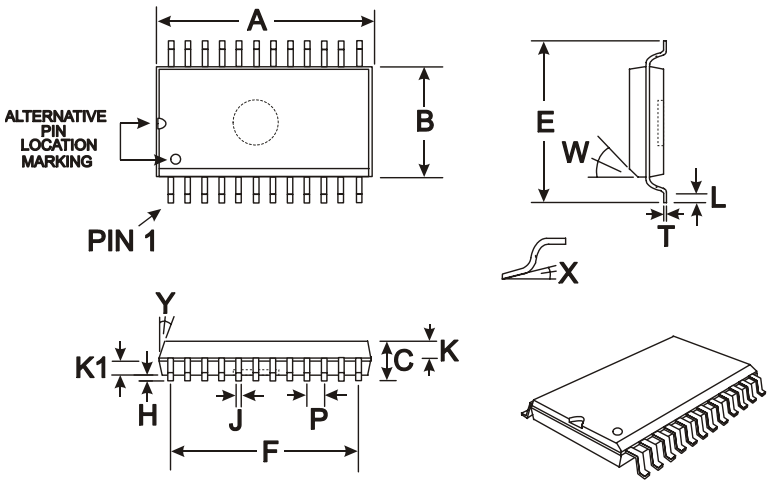


Figure 13 C-BUS Timing

8.2 Packaging



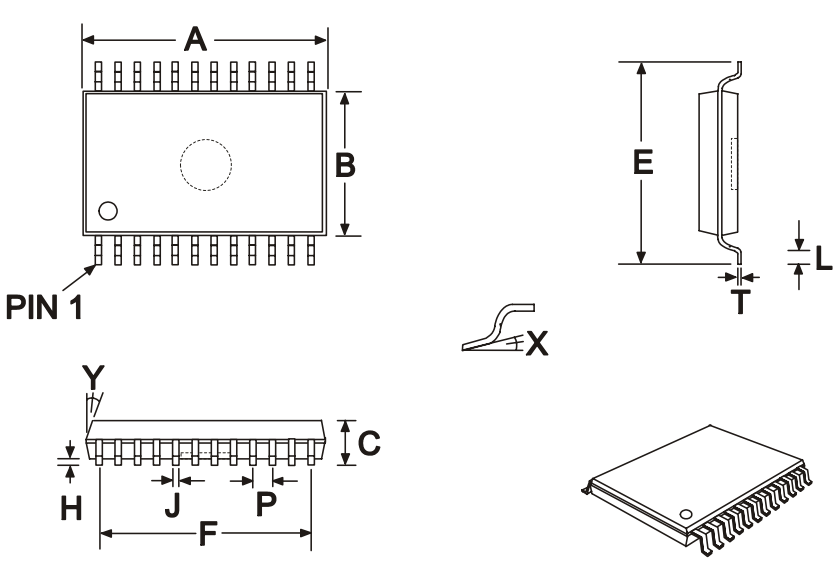
	DIM.	MIN.	TYP.	MAX.
*	A	0.597 (15.16)		0.613 (15.57)
*	B	0.286 (7.26)		0.299 (7.59)
	C	0.093 (2.36)		0.105 (2.67)
	E	0.390 (9.90)		0.419 (10.64)
	F		0.550 (14.1)	
	H	0.003 (0.08)		0.020 (0.51)
	J	0.013 (0.33)		0.020 (0.51)
	K		0.041 (1.04)	
	K1		0.041 (1.04)	
	L	0.016 (0.41)		0.050 (1.27)
	P		0.050 (1.27)	
	T	0.009 (0.23)		0.0125 (0.32)
	W		45°	
	X	0°		10°
	Y		7°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees
Co-Planarity of leads within 0.004" (0.1mm)

Figure 14a 24-pin SOIC (D2) Mechanical Outline: *Order as part no. CMX869AD2*



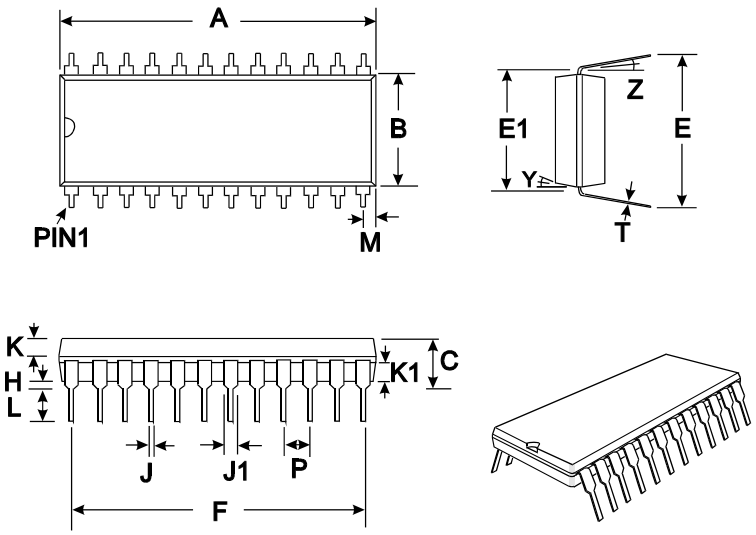
	DIM.	MIN.	TYP.	MAX.
*	A	7.70		7.90
*	B	4.30		4.50
	C	--------		1.20
	E	6.30		6.50
	F		7.15	
	H	0.05		0.15
	J	0.17		0.30
	L	0.45		0.75
	P		0.65	
	T	0.08		0.20
	X	0°		8°
	Y		12°	

NOTE :

* A & B are reference data and do not include mold deflash or protrusions.

All dimensions in mm
Angles are in degrees

Figure 14b 24-pin TSSOP (E2) Mechanical Outline: *Order as part no. CMX869AE2*



DIM.	MIN.	TYP.	MAX.
* A	1.200 (30.48)		1.270 (32.26)
* B	0.500 (12.70)		0.555 (14.10)
C	0.151 (3.84)		0.220 (5.59)
E	0.600 (15.24)		0.670 (17.02)
E1	0.590 (14.99)		0.625 (15.88)
F		1.10 (27.94)	
H	0.015 (0.38)		0.045 (1.14)
J	0.015 (0.38)		0.023 (0.58)
J1	0.040 (1.02)		0.065 (1.65)
K	0.066 (1.68)		0.074 (1.88)
K1	0.060 (1.52)		0.074 (1.88)
L	0.121 (3.07)		0.160 (4.06)
M		0.180 (4.58)	
P		0.100 (2.54)	
T	0.008 (0.20)		0.015 (0.38)
Y		7°	
Z		4°	

NOTE :

* A & B are reference datum's and do not include mold deflash or protrusions.

All dimensions in inches (mm.)
Angles are in degrees

Figure 14c 24-pin DIL (P4) Mechanical Outline: *Order as part no. CMX869AP4*

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